Instruction manual

PROM PROGRAMMER
Operation and Service

025-5500-11
REV A July 78

901-5500-11

DATA I/O

Programming systems for tomorrow... today

PROM PROGRAMMER
Operation and Service

025-5500-11
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1432 HeyLADD
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1433

OPERATING MANUAL
MODEL V

NOTE:

This manual reflects improvements in the Model V, including expansion of the memory to 4096 8 bit bytes and a higher speed system clock. Programmers containing these additional capabilities are identified on their rear panel nameplate by part number 901-5500-11, -12, or -13.

The expanded random access memory provides the programmer with the capability to program devices as large as 4096 x 8. To accomplish this update, a new RAM circuit card, a new address circuit card and a new MEU circuit card have been provided.

A significant increase in the programmer's system clock rate is an additional feature of the improvement package. Program cycle times have been substantially reduced while maintaining programming specifications. 2708 type devices, for example, which previously took over 5 minutes to program, can now be programmed in approximately 2 minutes. The time savings for larger devices is of course even more significant.

CAUTION

1. POWER ON/ OFF: DO NOT turn main power switch to either ON or OFF when PROMS are present in the PROGRAMMING Sockets. Device damage may result by programming A Junction during the power surge or decay.

2. PROGRAMMING LOGIC LEVELS: Data I/O convention states that a LIGHT on the display panel represents a PROGRAMMED JUNCTION (output indicators) or a bit to be programmed (input indicators).
Some devices Program to V_{oh} (HIGH) while others Program to V_{ol} (LOW). In order to properly program devices from a given data source, ensure that the selections of data inversion are properly made as follows:

   A. PAPER TAPE INPUT (701-1111 or 701-1112, Reader Driver Cards)
   Data read from Paper Tape normally displays a Light as a Programmed Junction for a hole detected in the Tape.
   The same is true from Parallel or Serial Remote Interfaces. If it is desired to reverse this relationship, the INVERT switch may be moved from Normal to Invert on the Input card (Reader Driver).

   B. TRANSLATED INPUT -- (701-1155 or 701-1117, 701-1138)

   HEX

   Data tapes of translatable format are accepted into all Data I/O Programmers. Program Data polarity may be inverted, in this case, by moving the Normal/Invert switch on the Hexidecimal Translator card to the Invert position.

   ASCII/BNPF

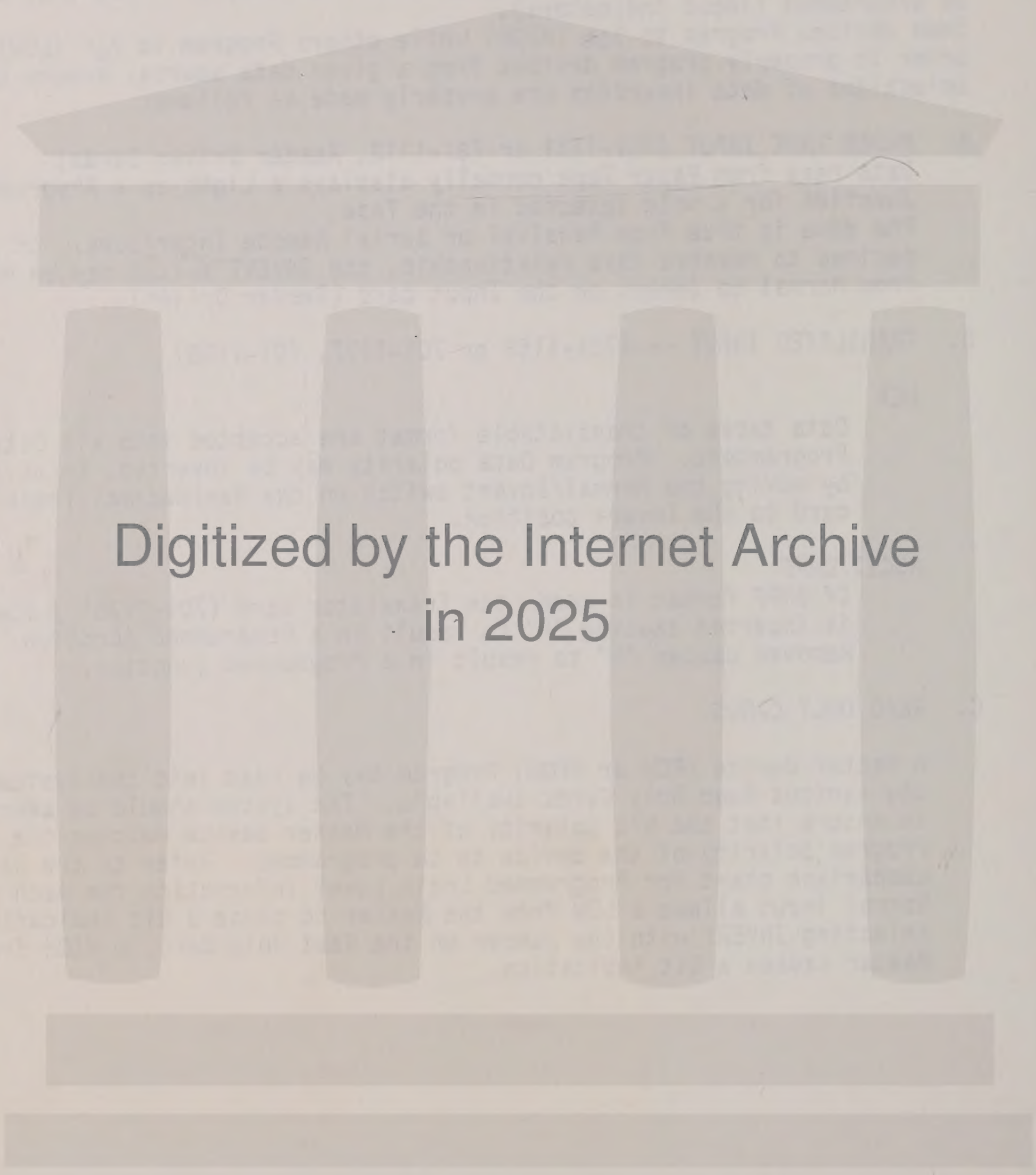
   If BNPF format is used, the Translator card (701-1138) jumper (JP3) is inserted causing "P" to result in a Programmed junction. JP3 Removed causes "N" to result in a Programmed junction.

   C. READ ONLY CARDS

   A Master device (ROM or PROM) Program may be read into the system via the various Read Only Cards available. The system should be exercised to ensure that the bit polarity of the Master device matches the Bit to Program polarity of the device to be programmed. Refer to the Data I/O comparison chart for Programmed Logic Level information for each PROM. Normal input allows a LOW from the Master to cause a Bit indication. By selecting INVERT with the jumper on the Read Only Card, a HIGH from the Master causes a Bit indication.

REFER TO THE APPROPRIATE OPERATING SECTIONS OF THE MANUAL(S) BEFORE ATTEMPTING ANY NEW OPERATION.

7/16/75



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INTRODUCTION

The Data I/O Programmers are designed as universal Programmers to program all commercially available Programmable Read Only Memory Devices.

The Model V Programmer is designed for engineering tasks requiring broad flexibility. It is also suited to certain field applications which require a portable instrument. Like its cousin, Model III, the Series V programmers also may be applied to volume production duties. This programmer contains automatic sequencing subroutines to allow complete testing, programming and verification of a PROM by a single operator function.

Options are available to allow input data to be derived from:

Paper Tape Reader (standard)

Mark Sense Card Reader

Computer Interface (Parallel)

RS232 Interface (Serial) with Translator

RAM Buffer (standard)

Binary Keyboard

Hexidecimal Keyboard

Octal Keyboard

Input Data Format conversions are abailable to allow ASCII character BNPF, BPNE, BHLF conversion, as well as Hexidecimal or Octal conversion options. The internal structure of the System is 8 Bit Binary.

Word Count Displays are available in 3 or 4-digit Decimal, Octal or Hexidecimal.

SECTION 1

OPERATING INSTRUCTIONS

1.1 GENERAL

The Model $\overline{V}$ contains interlocked mode selector switches on its Control Panel to allow the operator to select the desired input data source and recipient output with a single switch selection. Selection of mode may only occur when the programmer is in the STOP condition. This feature prevents the operator from inadvertently changing modes while the System is operating, thereby minimizing the possibility of operator induced error.

The RAM Buffer feature is offered as a standard 4096 x 8.

An integral 5 - 8 level, I-R Optical Paper Tape Reader is standard on Series $\overline{V}$ instruments. Also standard is one of three keyboards which must be specified at time of order: Binary, Hexidecimal, or Octal.

1.2 POWER SOURCE

The Model $\overline{V}$ operates from a power source of 105-135V, 50/60 Hz; or 210 - 250V, 50/60 Hz. Selection of High or Low power is done internally by a jumper assembly. A removable 3-conductor power cord allows power plug adaption for foreign power requirements without impacting the wiring of the internal system.

Power source selection is made at the factory at the time of shipment.

1.3 DISPLAY PANEL

1.3.1 Power Switch

Two switches are located on the Display Panel, namely, POWER ON/OFF (toggle) and RESET (pushbutton). Power is turned on to the entire System by moving the POWER switch to the ON (up) position. Power On indication will be evident by display lamps being illuminated.

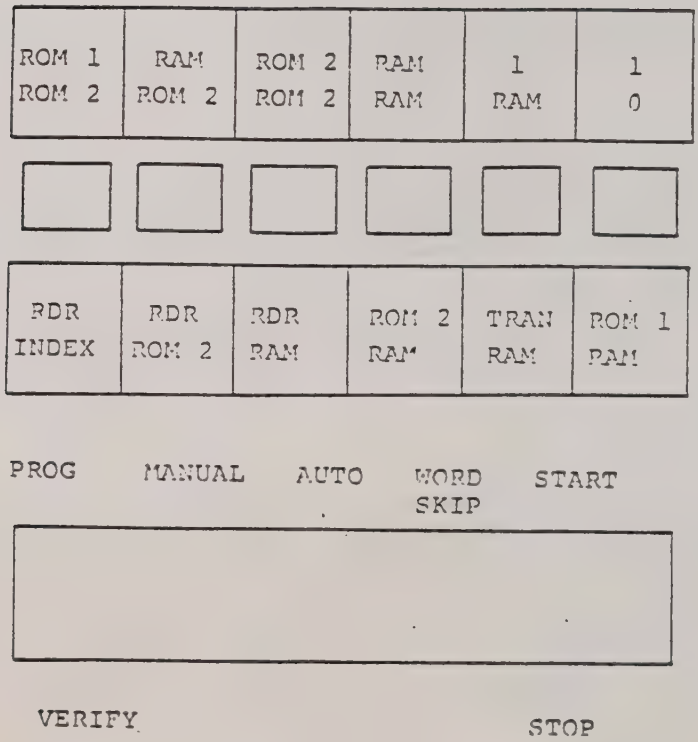
Power on automatically places the System into a (1) Reset state (Word Count Ø), (2) Stop, (3) Verify, (4) Manual. The status of the modes is clearly indicated.

1.3.2 Power Interrupt

The Display Panel contains a POWER INTERRUPT indicator, which turns ON at Power On, or at any other time in which power was lost for a period long enough to endanger the Data Integrity of the Integral RAM Buffer Memory. The indicator is cleared wnen START is enabled, and shall not again light unless power is lost and regained.

ILLUSTRATION I

MODEL V SERIES DISPLAY PANEL



1.3.3 Word Count Display

The Address of the internal system is displayed on the Front Panel by the Word Count Display. The standard Display contains three digits, to indicate the Address in decimal notation. The Expanded Address option adds another display to total four. This shall indicate a maximum word count of 4,095.

1.3.3.1 Octal Word Count

An option is available to display Address in Octal. If this feature is used, the Word Count contains four digits, to display up to 7777, indicating maximum Word Count.

1.3.3.2 Hexidecimal Word Count

An option is available to display Address in Hexidecimal. If this feature is used, the Word Count contains three digits, to display up to FFF, indicating maximum Word Count.

1.3.4 Direction Indicators

FORWARD and REVERSE indicators are used to inform the operator as to the direction the System is operating. In Manual operation, the direction may be changed by the FORWARD and REVERSE keys. In Automatic operation, the direction is automatically determined.

1.3.5 Programming Indicator

This indicator shall illuminate whenever a Write condition is commanded. It can only be seen when the programming speeds are slow enough to allow the indicator to turn On.

1.3.6 Reset Switch

This momentary pushbutton clears all operation to Stop, with Word Count becoming Ø. Address direction is simultaneously set to Forward.

1.3.7 Data A and B Indicators

These two indicators shall identify the word width (byte) applicable to the pROM to be Programmed. This data width is controlled by the Personality Card and is typically 4 (A channel), 8 (A plus B channel).

At the same time that data width is specified by the Program Cards, data length is also determined automatically. (See Section 1.5.)

1.3.8 Input Data Indicators

Eight LED indicators give the status of the eight bits of data to be selected input device. This means that the bit configuration is shown for the address indicated and will be the data to be programmed into the selected output device. PROGRAMMED BITS ARE ALWAYS INDICATED REGARDLESS OF THE SPECIFIC PROGRAM LOGIC BEING VOH OR VOL.

1.3.9 Output Data Indicators

Eight LED indicators give the status of the eight bits of data from the selected output device. The two rows of indicators, therefore, show comparison of data on both Buses.

1.4 CONTROL PANEL

The Control Panel of the basic Model V contains a row of six Mode Selector switches, a row of Function Control switches, and Manual Address Control Keys.

1.4.1 Mode Control

Six momentary level keys are used to select the entire I/O mission desired by a single motion. If, for example, ROM 1 to ROM 2 is desired, that key is depressed (toward the legend) illuminating the function legend. Mode selections may only be made when the instrument is in the STOP condition.

1.4.2 Function Control

Five momentary switch keys are used for control of the System with two being double function in nature.

1.4.2.1 Start/Stop

This single key initiates and terminates System operation. The action occurs upon releasing the key.

As START is depressed, all keys on the Control Panel are electrically locked out, except WORD SKIP and MANUAL.

1.4.2.2 Program/Verify

This single key selects the master function in which the machine is to operate. With PROGRAM selected, data is allowed to be written into RAM, ROM 2, or other output. In VERIFY, data is compared on the input and output selected devices, and if any mismatch occurs, the System shall hold and display the mismatch on the input and output line Bit indicators.

1.4.2.3 Manual/Auto

Two keys are used to select the function of MANUAL or AUTOMATIC.

MANUAL may be selected at any time, even if START is present. Manual mode causes a single cycle function, wherein the System shall pass through one complete sequence of operations and hold. A following cycle may then be initiated by use of the FORWARD and REVERSE keys.

The Keyboard section is activated when MANUAL is selected. The Keyboard input is disallowed in all AUTOMATIC modes.

In AUTO, the FORWARD and REVERSE keys are inhibited, and upon initiating START, the System shall perform one of three subroutines.

A. Verify

The System shall start at Word Count Ø, Verify forward to Word Limit (length selected by the Personality Card), Reverse, and Verify to Word Count Ø and cause Stop.

Any non-verify (compare) of input versus output data shall cause Hold and Display on the Address in which a non-verify occurs.

B. Programming pROM's (General Description)

The System shall perform three routines in sequence in any AUTO ROM2 Program Mode, Blank Check, Program Verify and then Stop. These sequences occur in Automatic operation, regardless of input selected.

BLANK CHECK is a test of the pROM to be programmed to ensure that it is indeed unprogrammed. If it is not data free, the System shall hold on Word Count location(s) where data appears, thus indicating Blank Check error.

The PROGRAM Mode indicator lamp normally turns off during Blank Check. If the System halts on an Address and displays programmed data bits, it indicates that the device was not blank and shows the exact data present in the pROM.

PROGRAM Mode shall automatically be selected following successful Blank Check. Program occurs to Word Limit and back to Ø, whereupon, Verify is selected automatically. Note: The Verify indication is not displayed during this automatic sequence.

VERIFY Mode is automatically selected following successful programming up and back to Word Count Ø. Verify is enabled to Word Limit and back to Ø, where Stop is commanded.

If Stop occurs in AUTOMATIC operation, it signifies that successful verification has occurred; after the successful completion of Blank Check and Programming.

C. Program of RAM

This mode shall not provide Blank Check, but only Program, Verify and Stop, in that order.

1.4.2.4 Word Skip

Word Skip is a means of stepping over an Address location, which does not Verify. In the AUTOMATIC mode, if Verify error causes halt, depression and release of WORD SKIP shall step over one Address location, and allow continuation of Verify. With MANUAL selected, depressing and holding the FORWARD or REVERSE key shall cause Word Skip as the WORD SKIP key is depressed and released.

if, during Automatic Programming of ROM 2, Blank Check detects data present in the pROM, depressing and releasing WORD SKIP shall bypass the remainder of the Blank Check operation. The instrument will then go automatically into the Program Mode.

1.4.2.5 Forward/Reverse Keys

With MANUAL selected, and START depressed, the single cycle operation of the System may be used with respect to Address and Data Clear functions Forward/Reverse.

The FORWARD and REVERSE keys shall cause repetitive (slew) operation when held down (after a 1/2 second delay).

1.4.2.6 Keyboard Section (See separate section "Keyboard Operating Instructions" for Details of Operation)
Series V instruments contain one of three Keyboards:

- Binary - Supplied on V (B) instruments for inputting data in Binary format.
- Hexidecimal - Supplied on V (H) instruments for inputting data in Hexidecimal format.
- Octal - Supplied on V (O) instruments for inputting data in Octal format.

In any MANUAL Program Mode where ROM 2 or RAM is the output selection, Keyboard data may be transferred to the input line. When FORWARD or ENTER keys are momentarily depressed, the input data will be transferred to the output line and the Address will step one. If RAM is the selected output, the Keyboard data will transfer to RAM in each step. If ROM 2 is the selected output, the data will be Programmed into the pROM in Socket 2, each step.

1.5 WORD LENGTH

The Word Length on the Model V is automatic, and is controlled by the Personality Card being used.

As an example, if a 32x8 Personality Card is used, the maximum Word Length is restricted to 31.

With MANUAL Mode selected, depressing the FORWARD key shall slew the Address and System operation up to 31. The Control System tries to move to 32, but is brought back to 31. If the Reader is selected, this feature can easily be seen as the Reader appears to buzz or oscillate at Word Limit.

1.6 CARD INSTALLATION AND CHANGE

Caution: Power should always be removed from the Programmer prior to installing or removing a circuit board from the instrument.

When power is removed, the contents of the RAM will be lost and must be reprogrammed prior to use.

Card changes are only necessary when changing Personality or Read Only Cards.

1.7 OPERATING INSTRUCTIONS

The following operating instructions are detailed in a step-by-step procedure so as to inform an operator of the affects of each function control.

It is assumed for all operations that power is turned ON.

1.7.1 Model V Series, Modes of Operation

- ROM 1/ ROM 2

  Used to copy the data from a Master ROM Socket 1 into a blank pROM in ROM Socket 2. It is assumed that the proper Read Only and Personality Cards are installed.

- RAM/ROM 2

  Used to Program or Verify the data from the RAM into ROM 2. This function is used usually following another input function such as KEYBOARD/RAM (RAM/RAM), RDR/RAM or Remote (IPT/RAM).

- ROM 2 / ROM 2

  Used normally for inspecting the contents of ROM 2, and may also be used for MANUAL Programming of ROM 2 from the input Keyboard.

- RAM/RAM

  Used normally for inspecting the contents of RAM, and also for MANUAL entry into RAM. MANUAL entry should be done in this mode so that Back-spacing or Reverse does not erase the prepared data.

- IPT/ROM 2

  This mode is used to input data to the ROM 2 via Translator from a Remote Location. May be used with options such as Parallel Interface, RS232 Interface, Mark Sense Reader, Etc, as well as Resident P/T Reader.

- IPT/RAM

  This mode is used for inputting data to RAM from any input source.

- Reader Index

  Used to find the beginning of a program. This is typically Word Zero (Ø). READER INDEX operates in two modes, MANUAL (Standard), AUTOMATIC (Optional).

- Reader/RAM
  Used to Program paper tape data into integral RAM Buffer Memory or Verify (compare) Reader data with RAM.

- Reader/ROM2
  Used to read data from the Reader, and directly Program or Verify a pROM in ROM 2 Socket.

- ROM 2/RAM
  Used to copy (Program) contents of ROM 2 into integral RAM Buffer or compare (Verify) ROM 2 with RAM.

- Tran/RAM (Translator PCC Optional)
  This mode uses the Translator Card option(s) to create an encoded word in RAM or Verify same. Standard options for this location include:

  BHLF (ASCII)
  BNPF (ASCII)
  ASCII - HEX
  ASCII - OCTAL

- ROM 1/RAM (Read Only PCC Optional)
  This mode is generally used for copy purposes, to Read a ROM into RAM for Verifying or Programming a pROM inserted into the ROM 2 Socket.

1.7.1.1 ROM 1/ROM 2 Program, Automatic

This operation is used to copy the data of a master in ROM Socket 1 into a blank pROM in ROM Socket 2. It is assumed that the proper Read Only and Personality Cards are installed in the instrument.

A. Momentarily depress mode select lever ROM 1/ROM 2. The lamp beneath the legend will indicate that the mode has been selected. Mode selection may only be made when the instrument is in Stop condition.

B. Place Master ROM in ROM 1 Socket.

C. Place blank pROM in ROM 2 Socket.

D. Select PROGRAM.

E. Select AUTO.

F. Depress RESET.

G. Depress and release START.

The System will Blank Check ROM 2 up to Word Limit and back to Ø. During Blank Check, the PROGRAM SELECT lamp will not illuminate.

Upon reaching Ø, the System shall start through the Program sequence and continue up to Word Limit and back to Ø. At this time, Verify* is automatically selected and Verify forward and reverse is accomplished.

Stop occurs upon reaching Ø, after a Verify has been successfully completed.

If the System halts with PROGRAM light Off, it is an indication that the ROM in Socket 2 is not blank.

If the System halts short of word zero (Ø) with the Program light On, the device (ROM 2) either Programmed or Verified incorrectly.

1.7.1.2 ROM 1/ ROM 2 Program, Manual

By selecting MANUAL and depressing START, incremental programming by Address location may be accomplished by depressing the FORWARD or REVERSE keys.

Word Limit may not be exceeded in either the Forward or Reverse direction. Automatic Blank Check is not performed in MANUAL.

Note: During all MANUAL modes, the FORWARD and REVERSE keys are dual function switches. For single entry, the key should be stroked firmly and released.

If the key is held depressed, after a time period of approximately 1/2 second, the SLEW or REPETITIVE CYCLE mode will occur.

1.7.1.3 Word Skip

WORD SKIP may be depressed to skip a single Address during Program or Verify. Often, if a device does not program correctly, if the hard to program location is skipped until the other locations have been programmed, the hard to program junction may program correctly on the reverse pass.

WORD SKIP may be used to bypass Blank Check in AUTOMATIC operations.

1.7.1.4 ROM 1/ROM 2 Verify, Automatic

This mode of operation is necessary only if a simple verification of two devices is desired. It is not required to Verify if Automatic Programming is used, as the final step was Verify in the AUTO mode sequence.

AUTOMATIC VERIFY, upon depressing START, shall Verify to Word Limit, and back to Ø Word Count and Stop. If Stop occurs, upon the Address reaching Ø, complete verification was successful.

1.7.1.5 ROM 1/ ROM 2 Verify, Manual

By selecting MANUAL and depressing START, each individual Address location may be incrementally verified by use of the FORWARD or REVERSE keys. Verification shall continue if correct to Word Limit; and if in error, shall halt on the error word and display the bits on the input and output lines.

* VERIFY mode being selected, in this automatic sequence of events, does not illuminate the VERIFY lamp.

1.7.1.6 RAM/ROM 2 Program, Automatic

This operation is used to program the contents of the RAM Buffer into ROM 2; it is assumed that the proper Personality Card is installed and cabled to the ROM 2 Socket. It is also assumed that the RAM has been programmed and the resident program has been verified.

A. Momentarily depress mode lever key RAM/ROM 2. The lamp beneath the legend shall illuminate. The instrument must be in Stop condition prior to selecting this mode.

B. Place blank PROM in ROM 2 Socket.

C. Select PROGRAM.

D. Select AUTO.

E. Depress RESET.

F. Depress and release START.

The System shall Blank Check ROM 2 up to Word Limit and back to Ø. During Blank Check, the PROGRAM SELECT lamp shall turn Off.

Upon reaching Ø, the System shall Program the PROM up to Word Limit, and back to Ø. At this time, Verify is selected and automatically verifies up to Word Limit and back to Ø. As Word Limit Ø is reached, Stop occurs, signifying that the complete Blank Check, Program and Verify sequences have been completed.

Note: Blank Check and/or Verify Override may occur by depressing WORD SKIP. Refer to Section 1.7.1.3.

1.7.1.7 RAM/ROM 2 Program, Manual

This operation is identical to Automatic (Section 1.7.1.6) except for MANUAL selection.

Upon depressing START, individual Address locations may be programmed by use of the FORWARD and REVERSE keys. Slewing shall occur up to Word Limit in Forward, and down to Ø in Reverse. This mode does not automatically Verify or Blank Check.

WORD SKIP may be used to override single Addresses.

1.7.1.8 RAM/ROM 2 Verify, Automatic

This operation is only used following a MANUAL Programming function. By selecting AUTO, VERIFY and START, the System shall verify the contents of RAM and ROM 2 up to Word Limit, back to Ø, and then Stop.

Stop indicates verification successfully completed.

1.7.1.9 RAM/ROM 2 Verify, Manual

This operation is used for inspection of data (comparing the contents of RAM with ROM 2).

A. Select VERIFY.

B. Select MANUAL.

C. Depress START.

Use either FORWARD or REVERSE keys for incremental or slew operation. Verification in Forward shall continue to Word Limit. Verification in Reverse shall continue to Ø Address. Any non-verify shall halt the System and display the bit contents of RAM on the input line, and ROM 2 on the output line.

1.7.1.10 ROM 2/ROM 2

This mode is used primarily for inspecting the contents of ROM 2. Occasionally this mode is used for Programming selected locations from the Keyboard.

A. Select mode by depressing the mode select lever ROM 2/ROM 2. The light beneath the legend shall illuminate. Selection must be made with the instrument in a Stop condition.

B. Select PROGRAM

C. Select MANUAL.

D. Depress START.

E. Use FORWARD or REVERSE keys to incrementally inspect the data content of ROM 2 on both lines of bit indicators. The Word Limit range defined by the Program Cards may not be exceeded.

F. Keyboard data may be Programmed into any location in a PROM, by simply entering the data into the input line by depressing the Keyboard keys desired, and striking the FORWARD or ENTRY key momentarily, to transfer the data into the PROM.

1.7.1.11 RAM/RAM

This operation is used for both inspecting and/or Programming via Keyboard, the contents of RAM. Inspection of RAM is normally done with MANUAL mode selected. Programming the RAM using Keyboard as the input is also accomplished in MANUAL.

It is assumed that the RAM has been programmed. Such sources as input/RAM, derived from Computer Card Reader; RS232 Input; or Paper Tape Reader are normally used for automatically programming the RAM.

- Depress mode select lever RAM/RAM. The light beneath the legend shall illuminate.
- Depress MANUAL.
- Depress PROGRAM.
- Depress and release START.

Inspection of the RAM Buffer contents may now be accomplished by using the FORWARD or REVERSE keys for changing Addresses.

The RAM data shall display in both Input and Output Data Bit Lines. When programming the RAM from the Keyboard, the RAM should be erased in the section(s) requiring a different program. This may be accomplished by striking the CLEAR key to erase data in one Address. Holding the CLEAR key down simultaneously with the FORWARD key will cause the System to slew and erase all data up to Word Length. To enter data, simply depress the desired key(s) for each Address and strike the FORWARD or ENTER key momentarily.

It is advisable to use the inspection procedure outlined above after the desired program has been entered into RAM - before using the RAM as a Programmer data source.

1.7.1.12 IPT/ROM 2

This mode is used to allow a remote input source to directly input data to ROM 2 via Translator, if used. The mode requires use of optional interfaces such as P/T Reader, MSCR, Computer Interface etc.

Each option is discussed under its own section.

To select the mode:

- Depress RESET. This ensures that Stop and Word Count ØØ is present.
- Depress IPT/ROM 2 mode lever. The lamp beneath the legend shall illuminate.
- Select PROGRAM (or VERIFY) mode of operation.
- Depress AUTO. Entry from remote input should be accomplished only in AUTO.
- Select the remote input device.

A. For Card Reader options, turn on Card Reader power.

B. For Computer Input Systems, the Computer or remote device shall enable select.

- Depress START. This shall enable Ready for all interface options, allowing data entry to occur.

As soon as data flow begins, the Word Count shall advance, and continue to do so up to Word Limit. At that time, the interface is inhibited. Verify after Program requires a Verify selection and re-input data.

1.7.1.13 IPT/RAM

This mode is used to access a Remote Input to RAM. It is used to enter data into the RAM (or Verify) from an external source. This mode requires use of an optional interface such as mark Sense Card Reader, Computer Interface, RS232 Interface, etc.

Each option is discussed under its own section.

To select the mode:

- Depress RESET. This ensures that Stop and Word Count ØØ is present.
- Depress I/RAM mode lever. The lamp beneath the legend shall illuminate.
- Select PROGRAM (or VERIFY) mode of operation.
- Depress AUTO. Entry from remote input should be accomplished only in AUTO.
- Select the remote input device.

A. For Card Reader options, turn on Card Reader power.

B. For Computer Input Systems, the Computer or remote device shall enable Select.

- Depress START. This shall enable Ready for all interface options, allowing data entry to occur.

As soon as data flow begins, the Word Count shall advance, and continue to do so up to Word Limit. At that time, the interface is inhibited. Verify after Program requires a Verify Selection and re-input data.

1.7.1.14 Reader Index

1.7.1.14.1 Reader Index, Automatic (Optional PCC Required)

To select this mode of operation, depress RESET to ensure that the System is in a Stop state. if START is On, modes may not be changed.

- Depress the mode select lever READER INDEX momentarily. The lamp beneath the legend will illuminate.
- Select PROGRAM by momentarily depressing the PROGRAM key. If the PROGRAM lamp is already On, omit this step.
- Select AUTOMATIC by depressing the AUTO key.
- Insert tape in the Reader, and locate the data portion of the tape at the rear of the Reader.
- Depress START. The START indicator shall illuminate, and the Reader shall move forward until the Beginning of Program is detected. At that time, the System shall halt with the STOP indicator On, and Word Count indicating Address Ø.

1.7.1.14.2 Reader Index, Manual

Depress MANUAL, then START. Hold the MANUAL key depressed throughout this entire sequence.

Depress the FORWARD key momentarily to single step, or hold down to slew. The Reader ONLY shall operate. Observe the Data Input lamps on the Control Panel. Use the FORWARD and REVERSE keys to step the tape to Word Zero (Ø) position.

Normally, a subword Zero (Ø) index is placed on the tape when it is prepared for Manual Indexing use. A good standard index is a "rubout" (all eight holes punched). This index is always placed on the tape one Address preceding the Word Zero (Ø) position of the tape.

Hold down MANUAL and step the tape forward using the FORWARD key until the subword Zero (Ø) index appears on the Input Data Display Line. Step forward one more step after the index appears. The tape is now positioned on true word Zero (Ø); release the MANUAL key.

The tape is now positioned so that the first word of the desired program is beneath the Read Head. DO NOT REMOVE TAPE, or change modes to other than Reader Input combinations. If the Reader is deselected, data index may be lost. Proceed with the next operation.

1.7.2 Reader/ROM 2 Program, Automatic

To select this mode of operation, depress RESET to ensure that the System is in a Stop state. If Start is On, modes may not be changed.

- Move the mode select lever READER/ROM 2 down momentarily. The lamp beneath the legend will illuminate, and all other mode lights will be Off.

  This action selects the Reader as an Input device and ROM 2 Socket as the Output device.

- Depress the PROGRAM key to illuminate the PROGRAM indicator. if PROGRAM is already selected, omit this step.

- Place the desired tape in the Reader. Beginning of Data must be located for either Verify or Program operations. This is accomplished in the Reader Index mode.

  After the tape is indexed by one of the methods described in section 1.7.1.14, proceed with the Programming operation as follows:

- Depress AUTOMATIC. This key action shall illuminate the AUTO legend and turn off MANUAL

- Depress RESET momentarily. This action initializes the System.

- Depress START. Programming will begin after Blank Check has been completed. The PROGRAM indicator turning On indicates that Blank Check is complete.

The Reader increments on each Word Count, after Blank Check. Programming speed is determined by the pROM being programmed. As Word Limit is reached, the System will reverse and program back to Word Count Zero (Ø). At this time, the System enters the VERIFY mode and proceeds to Verify (compare) the data in the Reader with ROM 2 up to Word Limit and back to Ø. As Ø is reached, the System stops. This signals the completed process. The Reader shall pass through four cycles in the Reader/ROM 2, AUTOMATIC mode, if all sequences are successfully performed, i.e.:

1. Program forward to Word Limit,
2. And back to Word Ø.
3. Verify forward to Word Limit,
4. And back to Word Ø.

If all sequences are successfully completed, the STOP indication appears, indicating that the pROM is Programmed and Verified.

1.7.2.1 Reader/ROM 2 Program, Manual

This mode is identical to AUTOMATIC in the selection of mode and locating the beginning of the Program Word.

This mode is used to Program step-by-step through a Data Field into a pROM in ROM 2 Socket.

After the mode has been selected, and the indexing is complete:

- Select MANUAL by depressing the MANUAL key.
- Depress RESET to ensure complete System initialization.

NOTE: MNOS devices erase before programming. RESET sets the initial Erase mode for MNOS

- Depress START. The START indicator shall illuminate.

The MANUAL keys are now available to step FORWARD or REVERSE.

Depressing the respective keys shall cause a single step if struck momentarily and shall cause slewing if held down over 1/2 second.

1.7.2.2 Reader/ROM 2 Verify, Automatic

This mode is identical to Programming in AUTOMATIC except that data from the Reader is only compared with the data from ROM 2 Socket. The Reader shall read Forward at maximum speed to Word Limit, Reverse and read back to Word Count Ø. If all Addresses Verify correctly, the STOP light shall hold at that point and display the Input Data (Reader) and Output Data (ROM 2).

- Selection of modes and functions may only occur when the STOP lamp is On. Therefore, to ensure Word Count Ø and Stop, depress RESET momentarily.

- Depress the mode select lever READER/ROM 2. The lamp beneath the legend shall illuminate.

- Depress VERIFY. This 2-function switch shall select VERIFY with one depression, and PROGRAM with the other. Ensure that VERIFY is ON.

- Select MANUAL.

- Select START.

To locate the first word of the data to be compared, Reader Index must be accomplished.

NOTE: If the Reader has not been moved since Programming in the same mode, Indexing is unnecessary.

Holding MANUAL depressed, use the FORWARD and REVERSE keys to increment the Reader. Observe the INPUT DATA indicators, and position the data up to the first word of data. Alternately, refer to sections 1.7.1.14 for standard and optional Reader Indexing methods.

- Release MANUAL.

- Depress RESET.

- Depress AUTOMATIC.

RESET was depressed to select STOP, and to ensure that Word Count Ø was present.

- Depress START.

Verification shall occur at maximum speed forward to Word Limit, and reverse to Word Count Ø. If complete verification occurred, the STOP lamp shall turn On and the Word Count shall read ØØ.

If an error occurred, the System shall hold on the non-verified word and display both Input Data (Reader) and Output Data (ROM 2).

1.7.2.3 Reader/ROM 2 Verify, Manual

This mode is identical to AUTO VERIFY in every respect except for selection of AUTO. MANUAL VERIFY is used to incrementally step through a program for visual and compare purposes.

1.7.3 Reader/RAM Program, Automatic

This mode is used to input a data tape into the optional RAM Buffer. The RAM need not be erased before programming as this function is accomplished automatically. To properly program the RAM, the Reader data must first be indexed to the first data location. Then, Automatic Programming and Verification occurs.

- Depress RESET. This action ensures that the STOP lamp is illuminated, to allow mode selection.
- Refer to section 1.7.1 for Reader Index procedures. After indexing tape, proceed with the following steps.
- Depress the mode lever RDR/RAM down momentarily. The lamp beneath the legend shall illuminate.
- Depress PROGRAM. This multifunction switch selects PROGRAM on one depression, and VERIFY on the other. Make sure that PROGRAM is turned On.
- Depress AUTO.
- Depress START.

The Reader shall move forward at maximum speed up to Word Limit, Reverse to Word Count Ø and repeat action.

The instrument is actually passing through a bi-directional Program cycle, followed by a bi-directional Verify cycle. As the Verify cycle is completed, Stop occurs, which indicates that verification of the programmed data is complete.

1.7.3.1 Reader/RAM Program, Manual

This mode is seldom used. Occasionally it may be useful to visually inspect the data as it is being read into the instrument.

The operation is set up the same as the Reader/RAM, Program AUTO, except:

1) Select MANUAL in lieu of AUTOMATIC.
2) Use the FORWARD and REVERSE keys to step through the Addresses after starting.

1.7.3.2 Reader/RAM Verify, Manual

This mode is seldom used. It may occasionally be useful to use this mode to inspect the contents of Reader data versus RAM incrementally. In this mode, no change of RAM may occur (inspection only is possible)

The set up is identical to Reader/RAM Program, Manual, section 1.7.3.1; except MANUAL is selected instead of AUTO.

The mode should only be used after the RAM has been programmed in one of the Reader/RAM modes.

The FORWARD - REVERSE keys are used to step and/or slew through the Addresses manually. Word Skip may be used to override any non-compare Address(es).

1.7.4 ROM 2- RAM Program, Automatic

This mode is used to load the contents of a Master ROM into the RAM for subsequent Programming, using the RAM as input.

The application is normally used in AUTOMATIC; however, there is no restriction as to MANUAL operation.

- Depress RESET. This ensures that Stop is present so that mode selection is possible.
- Depress mode select lever ROM 2/RAM momentarily. The lamp beneath the legend will illuminate.
- Depress AUTO.
- Place desired ROM into ROM 2 Socket location.
- Depress START momentarily.

The System shall Program the RAM from ROM 2, and Verify the data in both directions. If successful verification occurs, Stop shall illuminate at Word Count Ø.

1.7.4.1 ROM 2 - RAM Verify, Auto

This mode is used to Verify (compare) a Master ROM with RAM, and in some applications, completely test the output capability of a ROM after Programming (RAM/ROM 2).

The selection of mode is identical to 1.7.4 except that VERIFY is selected instead of PROGRAM.

When Start is initiated, VERIFY will occur up to Word Limit, and back to Word Count Ø. If successful verification is completed, STOP will illuminate at the end of the sequence.

1.7.4.2 ROM 2/RAM Program, Manual

This mode is seldom used. Occasionally it is useful for transferring a portion of, but not an entire tape program to RAM for subsequently programming a PROM using the RAM/ROM 2 mode.

Selection is identical to section 1.7.4 except that MANUAL is selected instead of AUTOMATIC.

- Depress START.
- The FORWARD - REVERSE keys are used. As the Addresses are changed, the data from the device in ROM 2 Socket will be programmed into RAM. Word Clear may be used to delete data from any Address(es) in the RAM.

  Word Limit (controlled by the Program Card installed in the Instrument) may not be exceeded.

1.7.4.3 ROM 2/RAM Verify, Manual

This mode is useful in observing the contents of ROM 2 versus RAM.

Selection is identical to section 1.7.4.1 except for Manual selection.

- Depress START.
- Using the FORWARD and REVERSE keys, the contents of ROM 2 is compared with RAM. Any non-compare shall cause the System to hold and display the words of each device.

1.7.5 Translator/RAM

This mode is optional, and is included in the manuals for the Systems which contain the feature.

1.7.6 ROM 1/RAM Auto/Program

This mode is used in Systems which have a Read Only Card. It is used to copy the contents of ROM 1 into RAM.

Selection and operation is identical to section 1.7.4 (ROM 2 - RAM) except that the mode lever ROM 1/RAM is depressed, and a Master ROM is inserted in ROM 1 Socket.

The usefulness of this mode lies in the fact that ROM 1 Socket is a "Protected Socket" when cabled to a Read Only Card, I.E., no Program Voltages may be applied through the Read Only Card and, therefore, no alteration of a Master PROM or destruction of a MASK ROM is possible.

1.8 PRINTED CIRCUIT CARD, INSTALLATION AND FUNCTIONS

The figure shown on the following page is a top view layout of the Printed Circuit Card modules. The following description briefly explains the function of each card.

NOTE: If any card is removed:

1) Make sure Power if OFF!

2) When inserting a card, verify that the component side of the card is facing the FRONT of the instrument.

1.8.1 Translator, PCC

This card position is normally empty. Translator cards are used with options of Hexidecimal or Octal Keyboard, or ASCII character formats are used.

1.8.2 Control Card, PCC

This card is the nerve center or processor of the System. It controls the selection of other cards for Mode Control, Read, Write and Verify functions; as well as Timing Generator and Speed Interlock functions.

The Control Card contains ROM's for intelligence, and is programmable to control specialized functions as required.

1.8.3 Address and Display, PCC

This card controls the location Address of all data words in RAM and ROM. It serves as the control center for determining Word Limit Control, conversion of information for Readable Display format, and Address pointer for all addressable functions.

1.8.4 RAM Buffer, PCC

The RAM (Random Access Memory) is the storage area for Data in the instrument.

Ram Buffer size is a standard 4096 x 8. The 8-bit configuration will serve both 8 and 4 bit device types automatically.

1.8.5 ROM 2, PCC

Most Personality Cards (Program Cards) are designed as 2-card sets. The Digital (often called the Program Control Card) is installed in the Digital ROM 2 Connector (Slot 6). The Analog (often called the Level/Data Interface Card) is cable connected to the Digital Card, and is inserted into the Analog ROM 2 (Slot 5) location.

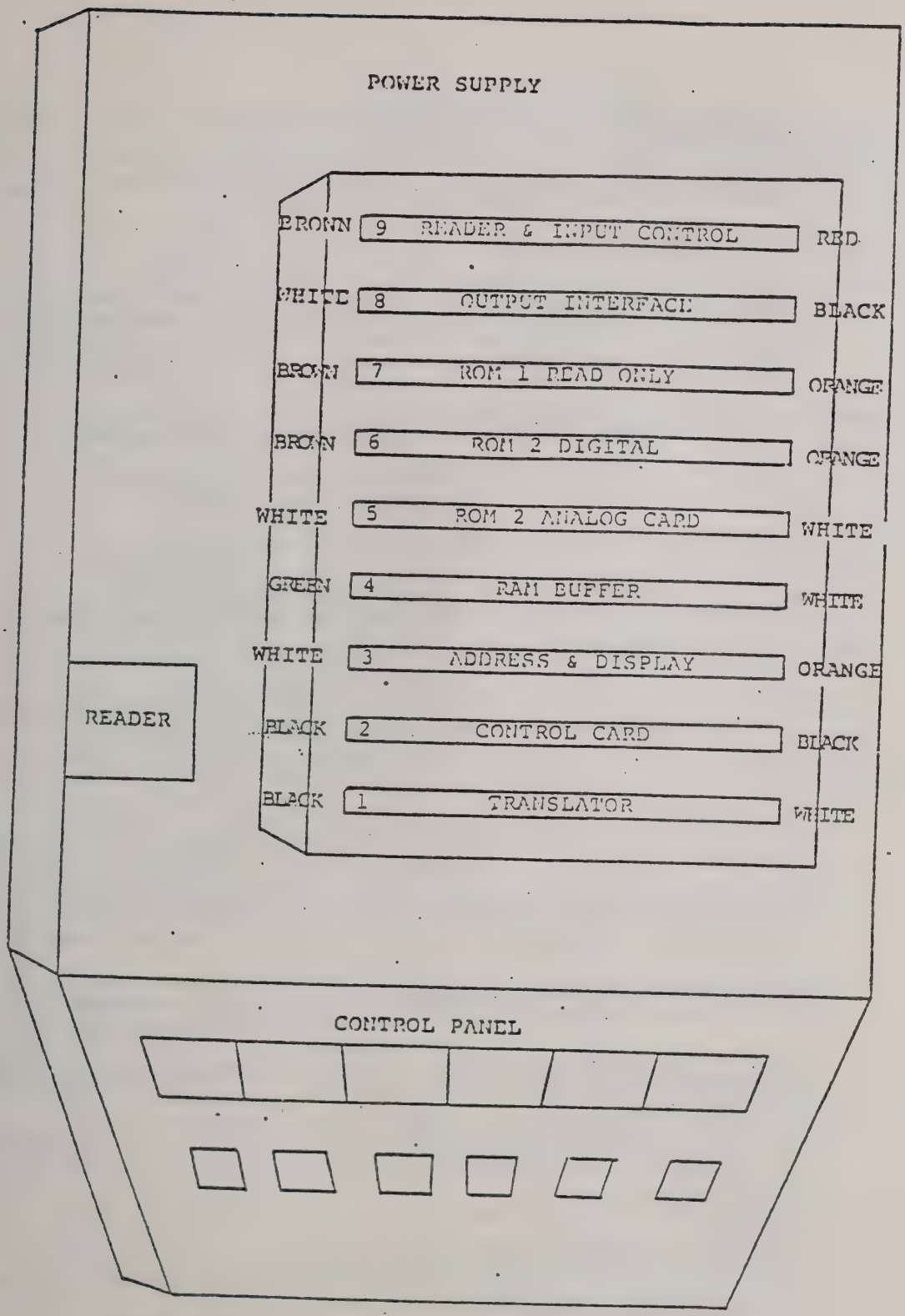

POWER SUPPLY
BROWN 9 READER & INPUT CONTROL RED
WHITE 8 OUTPUT INTERFACE BLACK
BROWN 7 ROM 1 READ ONLY ORANGE
BROWN 6 ROM 2 DIGITAL ORANGE
WHITE 5 ROM 2 ANALOG CARD WHITE
GREEN 4 RAM BUFFER WHITE
WHITE 3 ADDRESS & DISPLAY ORANGE
BLACK 2 CONTROL CARD BLACK
BLACK 1 TRANSLATOR WHITE
READER
CONTROL PANEL

Figure 1 - Top View Layout
Printed Circuit Card Modules

If the Personality Card is comprised of a single card, it is inserted into Digital ROM 2 (Slot 6) position.

A ribbon cable is routed from the Analog Card (or single Program Card where applicable), to the desired Programming Socket.

1.8.6 ROM 1 Read Only Card, PCC

This card is used to read Master ROM data directly from either RAM or a ROM inserted in Socket One (1) into a blank pROM inserted in Socket Two (2). Use of a Read Only Card provides a protected position wherein a Master PROM or Mask ROM cannot be accidently altered. The card has reading circuitry, but no writing privileges.

1.8.7 Output Interface, PCC (Card Design Defined by the Application)

This card is used for output devices, such as Remove Computer (full Duplex), device handlers or other output type units.

1.8.8 Reader and Input Control, PCC

This card is used to control the Paper Tape Reader and/or to control the Mark Sense Card Reader, Computer Interface, or RS232 Serial Interface.

1.9 KEYBOARD OPERATING INSTRUCTIONS

The Model $\overline{V}$ instrument may contain one of three manual entry techniques. Each technique is based on the users applications. They are:

1.9.1 Binary Input

The internal Bus structure of the Model $\overline{V}$ is Binary. The user who is used to programming and using devices in "machine language," (bit by bit format) should use the Binary entry Keyboard for manual preparation of data.

The Binary pad consists of eight Data keys "1 through 8," representing Bits 1 through 8 on the Data Bus. Depressing a Bit key shall turn on the appropriate Bit Indicator on the Display Panel.

The pad also incorporates an ENTER key, which is used to increment the Word Count only one position. No slew feature is used with ENTER.

The CLEAR key serves a Word Data Clear function, which is used to cancel the data content on the Input Data Register.

FORWARD and REVERSE keys are used for single entry when struck momentarily, and slewing when held down over 1/2 second.

1.9.2 Hexidecimal Input

This option is used by people who deal in "Hex" listings or software It allows a machine word (8 bits) to be constructed by two key stroke entries.

Hex data consists of Base 16 Binary, which is prepared by Ø-9 and A-F keys.

The Hex feature includes normal WORD CLEAR, FORWARD, and REVERSE keys, and also contains a 2-digit display, located directly above the keypad it indicates the data being entered, with shifting occurring to the left with each entry. FORWARD is normally used as the data entry (commit) key.

The 2-digit display is also used to Read the Hex data from the Bus. This feature is useful when playing back a program, to Verify the listing manually, and ensure that during the entry process (1) the Address(es) are data free before making entries, (2) That proper data is entered before committing it.

1.9.3 Octal Input

This option is used by people who deal in Octal listings or software. The feature allows the machine word (8 bits) to be constructed with three input key strokes.

The maximum data entry shall be 377.

The Octal keypad contains data entry keys Ø - 7, ENTER, WORD CLEAR and FORWARD/REVERSE.

The data is shifted left upon entering (MSD first) and the MSD is rolled off to 2 bits (Ø-3). If a higher entry is used than 3 for the MSD word, it will be cut off to Base 3, and displayed as such. As an example 5 shall become 1; 6 shall become 2 etc.

The feature contains a 3-Digit Display to "Read" the Octal data from the Bus. This feature is useful when playing back a Program, Verifying a listing manually, and to ensure that the next word location is blank before each entry is made.

1.9.4 Data Inversion (Octal or Hex)

Some pROM's require an inverted data structure for proper programming. The devices which program VOH, i.e., devices which come blank in "Ø", (Low) state.

The data preparation from the Keyboard may occur normally by selecting the Invert Position of the toggle switch, located on the Translator Card (Position 1).

The Key entry will display the same data as the representative key, but will invert the data to the instrument Bus. Playback is also inverted, so that the correct display remains for listing comparison.

1.9.5 Keyboard Operation Setup (Also see Sections 1.7.1.10 and 1.7.1.11)

Data is normally presented in to the RAM Buffer in MANUAL Mode when entering from the Keyboard.

To Program the RAM using any version Keyboard:

- Select PROGRAM
- RAM/RAM

- MANUAL.
- START.

Data may be resident in the RAM. In order to Clear the RAM for Manual entry, hold the Word Clear, and the FORWARD key depressed up to Word Limit.

- RESET.
- START.

The RAM is now Clear, and Data entry from the Keyboard will build a Data Record in RAM.

1.9.6 Verifying Keyboarded Data

After the desired Data has been entered into RAM:

- Depress RESET.
- Depress START.

By single stepping the Word Count with the FORWARD key, visual comparison of the RAM Program can be made with the code list (truth table).

1.9.7 Data Inversion

There are many applications where the input data from Remote Interface, Card Reader, Paper Tape, etc. needs to be inverted to Program different PROM devices. An example of this 32x8 pROM characterized by program logic VOH (High) versus another manufacturer's pROM which Programs VOL (Low). A tape prepared to Program VOH program logic pROM's must be inverted to program VOL program logic pROM's. A hole in the tape typically results in a corresponding programmed bit; without respect to the result of creating a VOH or VOL condition.

An INVERT switch is located on the Reader Drive Card to invert data coming from the Reader and thus allow the use of tapes prepared for one program logic to program pROM's of the opposite program logic. In the NORMAL selection, data will pass though the networks without alteration. If the switch is placed in the INVERT position, the data is complemented automatically.

The switch was purposefully put on the Drive Card, so that it is more difficult to reach than a Front Panel control. We hope that this will, in itself, prevent wrong or inverted entry of data without operator knowledge.

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SECTION 2

DETAIL DESCRIPTION

2.0 DETAIL DESCRIPTION

The following is a detailed description of all of the standardized components located in the MEU and Chassis area of the Model V Programmer. The standard cards do not include the programming cards or personality cards since each personality card contains its own supplement to the manual.

2.1 CONTROL PANEL

2.1.1 MODE SELECTION

The mode selection, accomplished by depressing a momentary lever switch on the Control Panel of the System, turns on an indicator, and issues a function address to the Control Card of the System to indicate the desired data routing sequence.

Mode selection may only occur in a STOPPED condition to disallow erroneous mode selection when a running or dedicated state is in motion.

Referring to the drawing entitled 1079, the six switches S1 through S6 are momentary lever switches which move in both directions for defining a Mode condition. Each switch has for its common or moveable contact, a driver which must be at ground (U3 Pin 10) in order to allow a Mode selection to occur. The A mode switches provide a ground level into the Mode Control ROM, U2, which acts as an input address. The output of the Mode Control ROM is presented as a Binary address to the 7442 decoder module, which feeds back to the input of the Mode Control ROM, to form a latch. The output address from the Mode ROM is also presented to the Control Panel as a source address, in order for the Control Card to then utilize this code to route the Input and Output functions properly in the system.

There are two rows of lamps to indicate the upper mode (DS1 through DS6) and a lower mode (DS7 through DS12). Each vertical row of lamps are common driven by a 75451 lamp driver through isolating diodes. Each horizontal row of lamps have a common driver Q1 and Q2 which provides 24 volt source power. The lamps are shut off or enabled by a Row Memory, U15 Pin 3 and Pin 6, forming a latching mechanism. As an example, if S1 were moved into the upper position, it would close contacts to allow a ground to be applied through the 7407 isolation amplifier onto the cable 1 address, driving the input of the Mode Control ROM, Pin 10. This will output an address from the Mode Control ROM of a nature so as to allow Pin 7 of the 7442 to become low, which feeds back to the Mode Control ROM to form a latch. The output address on A, B and C are then presented to

the front panel for proper data routing. In order for the lamp to properly illuminate, the same pin (Cable Pin 1) is presented to the lamp driver U9 Pin 1 and 2 which, when driven to ground, allows the output Pin 3 to become low. The only decision left to be made is to determine whether DS1 or DS7 will illuminate, and this is determined by the second half of the switch S1. Since the switch lever was moved upward, the "A" line was driven to ground. The A line is presented through the isolation amplifier U16 Pin 9 to drive U15 Pin 5 to ground on the Row Memory. This allows the output of the memory to provide a control line to the Control Card for selection address, and also drives the 7406 invertor U5 Pin 10 to ground, thereby turning on transistor Q2 for source power on the upper row of lamps. This then will allow the lamp DS1 to illuminate.

The same action is true for all six double action switches with the Row Memory conditioning the upper or lower row to be enabled and each switch being commonly "ORed" together to provide an input source address for mode control. In the lower left hand corner of the drawing, the mode program is shown which will indicate the input lines presented to the Control Card of the System for source address control.

2.1.2 FUNCTION CONTROL

2.1.2.1 DEBOUNCING NETWORK

In order for accurate multifunction control to be accomplished by a single switch such as START/STOP or PROGRAM/VERIFY, a DEBOUNCING NETWORK must be utilized so that any contact closure may not be acted upon unless it is truly intended. The darkened area on the following page of drawing 10798 indicates the DEBOUNCING NETWORK for the Control Panel. It is composed of a 74123 one shot multivibrator acting as a gated oscillator (U4 Pin 5). This oscillator has on its output, a line connected to second one shot, U4 Pin 2. Any switch closure for the PROGRAM/VERIFY (S7), WORD SKIP (S10) or START/STOP (S11) shall cause a ground to be presented to Pin 1of the timing one shot. This allows the output of U4 Pin 13 to become high, thereby releasing the clamp on the three toggles START Switch Memory, SKIP Control Memory and PROGRAM Switch Memory. As an example, if the START/STOP switch were depressed and a ground is presented on reference line C, the input ground shall be applied to U15 Pin 13 (START Switch Memory) and through the 7407 buffer amplifier U16 Pin 10 to enable the oneshot U4 Pin 1 to ground. Since the SELECT CLOCK is running, the one shot will retrigger as long as the switch is held in its depressed condition. This also allows the START Switch Memory to be set and remain in this set state until the switch is RELEASED. At that time, the one shot U4 Pin 13 shall expire on its normal time cycle; and when expired, shall cause the Switch Memory as well as the other two memories to return to a RESET state thereby, driving U15 Pin 8 High. The positive going line is applied to the Start Memory U7 Pin 3 which acts as a Binary and will SET or RESET on the release of the START/STOP switch and cause one action for each switch release accurately. As the Start Memory is set into

the START condition, the START lamp shall turn on via lamp driver U14 Pin 3 and this line becoming High releases the drive on buffer amplifier U3 Pin 10 (7407) which drives the common lines on all mode control switches, the PROGRAM/VERIFY switch and the AUTO switch. These functions therefore may not be altered when START occurs.

2.1.2.2 PROGRAM/VERIFY

The PROGRAM/VERIFY selection is identical to START with respect to the control of the PROGRAM Switch Memory U17 Pin 8 and the Program Memory Binary U8 Pin 6. Each depression and release of that switch S7 shall alter the Program Memory state. The lamp drivers U10 provide indication of Programming or Verification as conditioned by the state of the Program Memory. During the PROGRAM mode, if the Blank Check line, selected by the Control Card, becomes low, the output of the double inversion U5 Pin 12 will falsify the input to the Program lamp amplifier gate U10 Pin 1, turning off the lamp. If a Blank Check error occurs, the operator will know that it is in fact Blank Check, which is not correct.

2.1.2.3 AUTO/MANUAL

The AUTO/MANUAL Memory is manually toggled from SET to RESET conditions by the two switches S8 and S9 labled MANUAL and AUTO. AUTO may only be selected in a STOP condition where as MANUAL mode may be selected at any time. This condition is important in some PROM applications for indexing the Input Reader, or implementing a change in Data Word status when a keyboard is used. This single line, MANUAL, is presented through the interface connector J14 to the Control Card.

2.1.2.4 MANUAL DATA LINK OVERRIDE

The MANUAL switch is also presented to the Control Panel on the line SKIP DATA, which is J14 Pin 3. This is used as a DATA LINK OVERRIDE when held in the depressed condition, and using the FORWARD or REVERSE keys on the Control Panel. This will cause the Input Reader to move in either direction without regard to Address which is inhibited from operating as in the PROGRAM function and WORD LIMIT. The entire Control Panel is interfaced to the MEU by the 16 Pin connector J14.

2.2 CONTROL CARD

The Control Card is the sequential allocator or processor of the programmer. It is the heart of all decision making for go or no go status, START or STOP control and AUTOMATIC mode selection. It is basically divided into five sections which are CLOCK and TIMING, MANUAL TIMING, DATA REGISTER and VERIFY, MODE CONTROL, AUTO mode selection.

2.2.1 CLOCK AND TIMING

Referring to the drawing (1078C), the Master Clock, U14 Pin 3, will only run when the input network of Input and Output Busy Gate, Clock Inhibit Line and Cycle Hold Memory are all in a High Condition. At that time, the Master Clock is a free running oscillator, which applies a negative going pulse into an invertor, U16 Pin 1, which drives the Clock Generator, U27 Pin 5. Figure 1 on the following page shows the clock timing relationships wherein the master clock is a negative going pulse of a speed of approximately 100 KHz. It is applied through a Timing Clock Generator for a divide by two squarewave, with output on U27 Pin 5. It can be seen by the Timing Diagram that the negative area of the Clock Generator is the Chip Enable period in which the Program PROM's A & B (U3 & U4) on the schematic are enabled. During this time the Address Register is in a Stable or Static condition, thereby inputting an Address; and when Chip Enable is brought to low, the respective Data Words on the outputs of both ROM's are presented to the Logic and Control section. The routing or decision making of the following Address which is utilized from each control ROM is derived by the Program B ROM U4.

The first four lines PINs 1, 2, 3 and 4 of the ROM are presented to the data inputs of the Address Register, which are tested on the positive going edge of the Clock Generator (Figure 1). In this way, the Register is updated at the trailing edge of each Chip Enable line so that the Address is pre-prepared into the PROM's for minimum impact of rippling. The following three lines shown on the Timing Diagram labled Input Busy Test, Read and Output Busy Test show that there is a space between pulses which represents the time period which is allowed for the Address Register to set up the next Address location commanded from the PROM. All lines from the PROM's are open collector type terminations, so that they are wire "orable" without damage. All lines will drive low for a bit, so that it is easy to understand the actual Timing operation of the System.

2.2.2 CYCLE HOLD

Cycle Hold Memory clears on each Clock cycle in the MANUAL mode of operation, which is shown at the bottom of the Timing Diagram, Figure 1. The Output Busy Test pulse is applied to the Manual Stop Gate, U6 Pin 4, whose output is U6 Pin 6. (Diagram on following Page) As the pulse becomes high on the input U6 Pin 4, the output of the gate becomes low. A Filter Network composed of R29 and C6 hold the output of the gate low for a short period after the inputs to that gate are falsified, as is shown on the figure by the Integrating Network R29 and C6. Since the output of the gate is low, which is presented to the following gate U9 Pin 5; when U9 Pin 4 becomes low, a narrow pulse is applied through that gate to provide a reset pulse to the Cycle Hold Memory. The Memory, becoming low, drives the diode CR4, which clamps the Clock Timing Network on U14 Pin 7 to stop the Clock until the next start command occurs either by Manual Start or Manual Keyboard Entry.

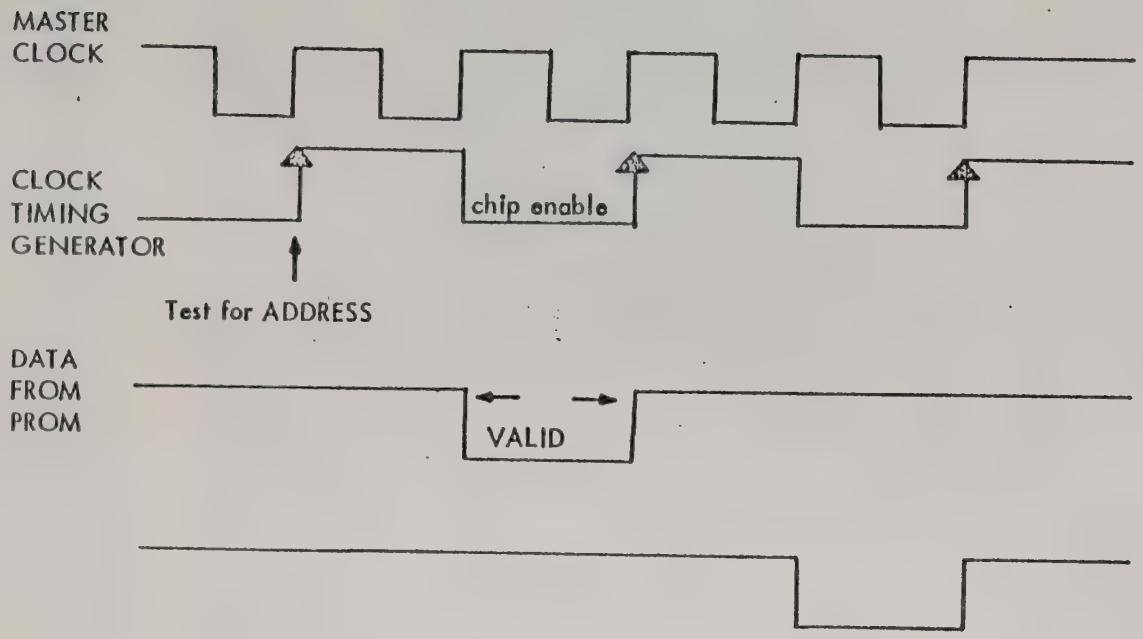

FIGURE 1
CYCLE TIMING

The output data routing of PROM A and B for control in sequential function management will be dicussed under the appropriate heading to fully define the entire function. Normally, however, this System is programmed so as to test for Input Busy of all input devices, then Read Data to bring the character into the Control Card, test for Output Busy, Program and then Verify. Following successful Verification, the Address is incremented to the next location and the process is repeated. Jump conditions are available for Translator, Word Limit and other functions, which require special recognition under their appropriate heading, therefore, each line will be discussed separately.

2.2.3 MANUAL CLOCK OPERATION

Referring to the schematic (008-1078), the Manual Entry Clock Clock Control is shown. In the lower right hand corner of the drawing, three terminals LL, KK and E are shown. LL and KK are the FORWARD and REVERSE keys on the Control Panel, which are presented through the 7408 Or Gate, which is then gated with Space Bar, so that any one of the three functions occuring, will cause the output of U6 Pin 3 to become high. This action allows the NE555 Clock to begin operation as soon as the RC Filter Network has been charged to a high state. The first clock pulse out, with Pin 3 becoming high, passes through the RC Coupling Network C21 and R38. This positive going pulse is applied through the Nor Gate U18 pin 3 to set the Cycle Hold Memory to On. This action initiates a single Clock function of the timing and control previously defined. The Clock cycle of the Clock Timer, U21, is approximately 500 milliseconds, which allows a charge through capacitor C23, R43 and R44. As soon as the Clock has expired and fired once again, the Slew Memory will set. As the Slew Memory sets, it drives the 7407 U20 Pin 8 to Off or High. The effect of this action then allows the 30K resistor R41 to be placed in parallel with the 330K resistor R44. This causes an increase in speed of the Timer for Slew operation.

The net effect of this Timing Network is that when a FORWARD or REVERSE key is depressed and held down, a pulse will be initiated immediately to start one cycle of operation of the System. A half second pause is then spanned before Slew operation begins. This allows the operator to single step by striking a key firmly and releasing the key prior to a half second interval for single step operation of the machine, or by holding the key down, slewing may occur.

2.2.4 POWER INTERRUPT

The Power Interrupt Memory, U11 Pin 11, is set to an On state with power on. This occurs because the 100MFD capacitor C1 represents a low impedence in a discharged state, and as power is first turned on, allows the Power Interrupt Memory to set to a high state on Pin 11. This capacitor also is coupled through the buffer, U1 Pin 4, to cause system Reset at power on time. As soon as the first Start command has occured, the Power Interrupt Memory shall clear, turning off the indicator on the Control Panel.

2.2.5 SPACE BAR OPERATION

The SPACE BAR or ENTRY key is a single cycle function only. This means that unlike the FORWARD and REVERSE keys, as the SPACE BAR is depressed, it simply creates one Clock cycle; therefore, the Timer itself does not repetitively fire. This occurs because of the 7407, U20 Pin 5, applying a ground across the timing capacitor C23, which disallows the Timer to charge and reset itself.

2.2.6 DATA REGISTER

The Data Register is composed of eight type D flip-flop Memories, which allow a data transfer from the DO Buss to the DI Buss on the Main Electronics Unit (MEU). The purpose of the Data Register is to hold the data which was presented from an input device, which may only occur on a momentary basis; and present that data then as a memory condition to an Output device such as a PROM to be programmed, output to Computer or RAM. The data is presented to the Data Register during the Read cycle; and slightly after the leading edge of the Read cycle, the Data Register is tested. Figure 2 on the following page shows the timing relationships of the Master Clock (U14 Pin 3), the Clock Generator (U27 Pin 5) and the Read Pulse, Data Load Pulse, Data Register and Data on the DO Buss. It can be seen that the Clock Generator changes state on the negative going edge of the Master Clock. During the low time of the Clock Generator, Chip Enable to the Timing and Control ROMs is issued; and it is during this time that the Read Command is issued from U3 Pin 4 as a low going pulse. This pulse is presented through the Strobe Gate, U2 Pin 6, whose other input (Pin 5) is a disable line for Blank Check functions; which will be discussed under that appropriate heading.

The output of the Strobe Gate is applied to the external Pin X which tests the Input Device for data content. The data is placed then on the DO Buss during the Read cycle as is shown on Figure 2 at the bottom of the figure where zero or low equals a bit. After the Clock cycle becomes high (Master Clock U14 Pin 3), the high going pulse enables the Data Load Gate, U8 Pin 9. The output of the Data Load Gate, therefore, is presented to all Clock inputs of the Data Register; which takes the information from the DO Buss and memorizes that data, and places it on the DI Buss. At the end of the Read cycle, the input device (such as Paper Tape Reader) is deselected from its Data Input Network; and therefore, only other information such as RAM, PROM or whatever information is then available on the Buss for display.

Following the Read cycle, normal timing in the Control Card consists of checking for Output Device Busy; and if a Busy condition does not exist, the next logical step will be write which is Program from data on the DI Buss to the selected output device.

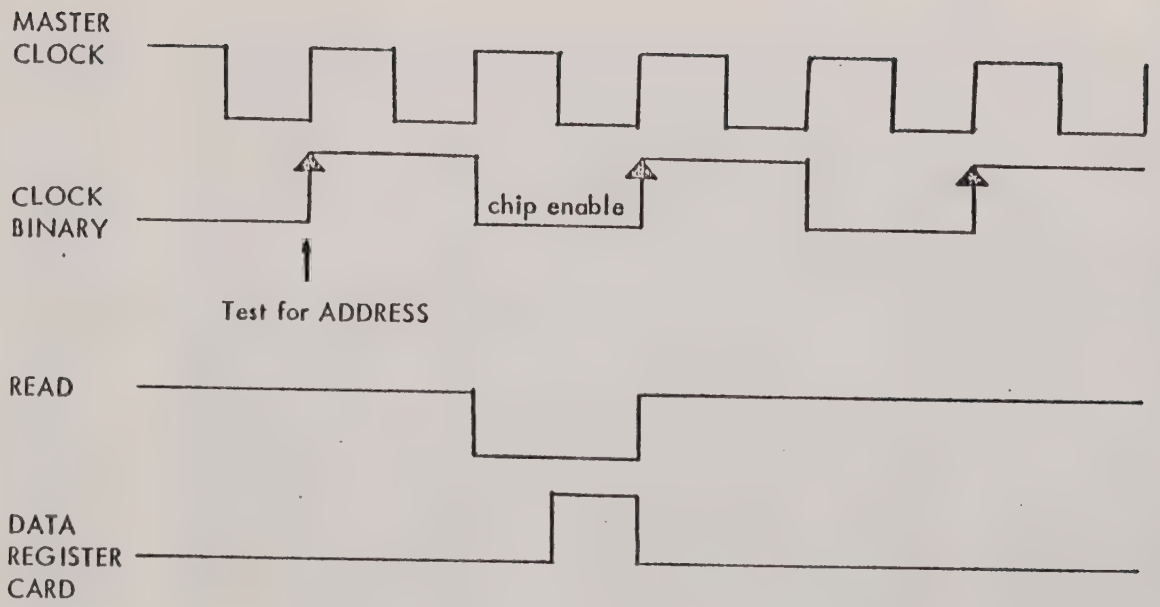

FIGURE 2
CYCLE TIMING

2.2.7 VERIFICATION

The information presented on the DO Buss and the data contained in the Data Register are gated together for verification in two bytes, namely high order and low order. The high and low order bytes are divided, and are enabled by the A inhibit line and B inhibit line arriving on Pin 19 and W on the left hand side of the drawing. An Enable is a low or ground which is controlled by the Personality Card involved. Some Personality Cards utilize four bit low order information, while others require eight bit information, and others yet require four bit high order information. Therefore, complete flexibility on the Control Card exists on Compare by investigating only the high or low order sector selected by the Personality Card involved. The output of the High and Low Order Error Gates are presented to the Verify Error Gate, U16 Pin 13, wherein an error is a high condition. At the time Verify is tested from the Control Program A PROM, the pulse exiting on Pin 3 of U3 turns off invertor U5 Pin 4 so that the V line drives the Verify Error Gate U6 Pin 12. If an error had existed, the output of U1-11 shall cause the Address Register to set to a minus one condition. This will then cause a repeat of the existing function of Output Busy Test, Write and Re-Verify. That loop will be maintained until proper verification occurs; and until that happens no incrementing of address is possible. The program flow diagram on the following page, shows the jump procedure and flow rules of the Control Card.

2.2.8 WORD SKIP

Word Skip disables the Control Card for both Reading data for Verification purposes and Writing until the next Address has been reached. The Word Skip function is enabled by the Control Panel key WORD SKIP, and will remain in a low condition until the Address is incremented by 1; which will then clear the Word Skip Memory on the Control Panel. As long as the ground is maintained on the Word Skip line, Pin 33, Programming and Verification is inhibited.

2.2.9 MANUAL DATA ENTRY

Keyboard information is presented through the K1-K8 lines located at the lower left hand corner of the drawing. Individual lines may set the Data Register bit by bit or a word at a time depending upon the Keyboard option device being used. The Keyboard input is normally only available when MANUAL is selected and START is depressed. WORD CLEAR is another key on the Control Panel that is used to manually clear the Data Register. It is a ground or low going pulse arriving on Pin 5 in the upper left hand corner of the drawing.

2.2.10 INCREMENT ADDRESS AND INPUT CONTROL

Two gates are used on the Control Card to separate the Input Advance and Increment Address functions. They are controlled by the ROM U3 Pin 5 and 6. The reason for the separation of functions is to allow the input device to step under control of the Control Card during multicode sequence functions. Functions such as BNPF translator or other automatic translation formats allow the input device to move without incrementing the Address. The Address will then only be incremented at a controlled time period.

2.3.0 DISPLAY PANEL

2.3.1 POWER INTERRUPT

The Power Interrupt line arriving on Pin 19 will turn on the Power Interrupt Pulser, U7, when the Memory on the Control Card is in the set or high state. This turns on a Free Running Pulser, U7, which drives through Inverter, U3 Pin 8, to blink the POWER INTERRUPT indicator on and off. The POWER INTERRUPT indicator will remain in its blinking condition until START is depressed on the Model III or V Control Panel, thereby clearing the Power Interrupt Memory on the Control Card.

2.3.2 DIRECTION CONTROL

A Single Input Line Forward, Pin 21, illuminates the FORWARD indicator in one condition and the REVERSE indicator in the second condition by the single and double Inverters, U3 Pin 4 and 6.

2.3.3 OPTIONS FOR ADDRESS AND DISPLAY

2.3.3.1 HEXIDECIMAL DISPLAY

The jumper JP1, located at the top of drawing number 1048A, when inserted, will allow the HP7340 devices to be used for displaying hexidecimal Address. This requires a Hexidecimal Address Display Card, part number 701-1432, which is a standard option for the System.

2.3.3.2 HEX/OCTAL ADDRESS CARD 1432

Referring to the Hex/Octal Address Card, 701-1432, at the end of this manual, it can be seen that the difference between this Address Card and part number 1431 is the Data Conversion feature. The Address Counter, as well as the Output Data Buffers, are identical to the 1431 card, however, the data outputs from the Address Counter are applied into four 74157 devices with outputs which directly drive the display. The 74157 devices are arranged in such a manner that they will display in either Hex or Octal format conditioned by Jumper JP3. All other functions on this card remain identical to the 1431. This Hex/Octal Address Card may drive the Word Count in Octal format by using the 1048A Board with 7300 or 7340 devices, however, in Hexidecimal the 1048 Board must utilize 7340 devices to properly display in Hexidecimal Word Count.

2.4 INPUT CONTROL

Two input printed circuit cards are used in the Model III or Model V systems. One being used for Paper Tape Reader or Mark Sense Card Reader Input, and the second being used for Paper Tape Reader or Remote Parallel Data Input.

The 1111 card is the basic Reader Driver Board shown at the end of the service manual, which allows either Paper Tape Input or Card Reader Input, a standard card, which is capable of being used in either the I, II, III, or V Model Programmers. Referring to this diagram, selection for Input occurs on the lower left hand corner of the drawing at Pin F labeled Model III Reader Select. This line, becoming low, and the ENABLE switch on the side of the Reader in the center position, allows the Select Buss to

become high. This will then release the clamp on the Data Output Gates via U15 Pin 8 becoming open and enable the Coil Driver Advance Gates U13. Input advance occurs by the Address line, Pin 17, becoming high. This line enables the Strobe Delay and Busy Delay one shots with the leading edge of the Strobe Delay testing the Direction Memory for the desired direction of count steered by the input line Pin 13 labeled Direction. The trailing edge of the Strobe Delay enables the Reader Advance Counter so that it will increment either Forward or Reverse as dictated by the selection of the Direction Memory. The Advance Counter is a Johnson type Counter which is used for driving the four coils on the Paper Tape Reader for detent incremented motion. The data from the Reader is applied from the LED photo transistors to the input lines S through Z in the upperleft hand corner of the drawing, through Reader Data Preamplifiers and then presented to the Data Invert gates U8 and U2. Data may be applied in either the true or complement form as dictated by the selection of the Data Invert Switch, S1. The output of the Data Invert gates are, therefore, presented to the Data Output gates U3 and U9, which are tested by the Read pulse arriving on Pin P in a positive direction. The data out of the Data Output gates is a low going level the width of the Read pulse, which are presented directly on the DO BUS lines to the Control Card of the System.

The Busy Delay, adjusted to approximately seven milliseconds, drives the Busy Line, Pin N, high during a Busy condition. The purpose of the Busy Delay is to stop the Control System of the MEU while the Reader is advancing to the next incremented position. The data must become stable before the Busy Delay allows a clocking of the Control Card to continue.

2.4.1 CARD READER OPTION INPUT

Data from the Card Reader is presented through the J1 connector by turning on the remote Card Reader, which grounds J1 Pin 5. This action will turn off the transistor which releases the LED power enable applied to Pin 18 of the card. This pin drives the LED'S on the Photo Reader which in effect turn all LED'S off, which disables the Reader Data Preamplifiers U7 and U1. Card Reader selection becoming ground on Pin 5 also disables the Busy Delay, U12, and cuts off inverter U4 Pin 6, located in the center of the drawing. As soon as this occurs, the Strobe Memory, U6 Pin 8, is reset or high; and the Card Reader is selected, the Busy Gate CR Busy, U10 Pin 11, allows the Busy Line to become busy, thereby shuting off the Control Card Clock. It will remain stopped until a Strobe arrives at the input of the System on Pin 4 of J1. The leading edge of Strobe will set the Strobe Memory to On, which releases the Busy Line of the System by falsifying the CR Busy Gate, U10 Pin 13. The Control Card is now activated which takes the information presented and paralleled with the Reader Data Preamplifiers from the Card Reader itself, and tests that data through the Data Output Gates and presents it to the DO Buss. As soon as the Control Card has accepted the data, and the Address is incremented, the leading edge of the Address Pulse clears the Strobe Memory, thereby causing the Buss to become busy once again and stopping the Clock. This action will occur until each input Strobe Pulse, which is applied to the CR Counter U11 Pin 11 counts the Counter to position 32. As position 32 is reached, the output DO of Counter U5 drives transistor Q1 off the approximately 200 milliseconds. This line, labeled Busy,

clears the Strobe Memory, and drives the Busy Line busy through Inverter, U4 Pin 10. This will cause the Control section to halt until the Busy Line is cleared so that the card which was passing through the Card Reader may exit from the Card Reader, thereby dropping Card Present Line and resetting the 32 position Counter.

For proper operation, the Card Reader input is implemented in either the PROGRAM or VERIFY mode by selecting AUTOMATIC and READER to RAM mode of operation. When a card has been read into the System, the Word Count shall read 32 or increments thereof.

2.4.2 INPUT PAPER TAPE OR PARALLEL REMOTE INPUT CARD, 1112

This Printed Circuit Card is used when parallel input options are required other than Mark Sense Card Readers. It is a standard card which is capable of being used in any Model I, II, III, or V Data I/O Programmer and may be used with remote Computer input or any other Busy/Ready type interface for presenting data to The system for recording in ROM or RAM devices.

2.4.2.1 SELECTION

Selection of input occurs on Pin F located in the left center of the drawing which arrives from the Control Card of the Model III or V Control System. This low level is applied to two Inverters U10 Pin 1 and 3, and Select gate U22 Pin 9. The purpose of U22 Pin 9 Select gate is to release the clamp on the Data Read Out gates so that information may be presented to the Buss at Read Pulse time. Inverter, U10 Pin 2, is used as a gated selection for Data Selectors to select the source of information from either Remote Parallel Input or Reader Data Input. The Inverter, U10 Pin 4, is used to release the clamp on the Reader Advance gates and drives when the center position of the Reader Switch is reached, allowing Pin K to also become high.

2.4.2.2 INPUT ADVANCE

The Address Line, Pin 17, located on the right lower center of the drawing, arrives with its positive edge or leading edge triggering the Strobe Delay U17 Pin 2. The leading edge of the Strobe Delay tests the Direction Memory and sets it in the direction as steered by the Direction Input Line, Pin 13. The Direction Memory simply steers the Direction Control Gates U21 Pin 1 and 5 for the Johnson Counter (Reader Advance Counter) to increment or decrement on the trailing edge of the Strobe Delay. As soon as the Strobe Delay is placed in motion and Pin 4 becomes low, the Busy Delay U17 Pin 12 becomes low or Busy for approximately seven milliseconds. This drives the Buss Pin N low or busy during that period so that the next Data Input Busy test will cause the Control Card to lock up or hold until the busy time is spanned, thereby allowing the data to become stable at the input terminals of the System once again.

2.4.2.3 READER DATA

Data from the Reader is presented through the terminals in the upper left hand corner of the drawing labeled S through Z, through 9818 preamplifiers and are then presented to Data Selectors U7 and U6. The Data Selectors are 74157

1982 DATA I/O COMPARISON CHART OF PROGRAMMABLE DEVICES

MOS PROMS

Array	Technology	Pinout	Device	Logic Level	Card Set	Rev.	Socket Adapter	Unipak	Mospak	Gang Module	Rev.	Characterizer	Model 16	Model 120/121	Family	Pinout
Advanced Micro Devices					DATA I/O Part Numbers											
	256x8 MOS	24	1702/AM9702	VOL TS	1183-1	C	1047	-	-	-	-	-	-			
	256x8 MOS	24	1702A-AM9702A	VOH TS	1183-1	C	1047	-	-	-	-	-	-			
	1024x8 MOS	24	2708/AM9708	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**	21	27
	2048x8 MOS	24	4716/AM9716	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	**	19	23
	4096x8 MOS	24	2732/AM9732	VOL TS	1512	C	1531	A	D	0075	F	1572	1705	**	19	24
	8192x8 MOS	28	2764/AM9764	VOL TS	1512	A	1622-001	F	E	0074	A	1564-001	0042	**	35	33
American Microsystems Inc					DATA I/O Part Numbers											
	512x8 MOS	24	S9834	VOH TS	1230-1	B	1033	-	-	-	-	-	-			
	512x8 MOS	24	S5204A	VOH TS	1230-1	B	1038	-	-	-	-	-	-			
Electronic Arrays					DATA I/O Part Numbers											
	1024x8 MOS	24	2708	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**	21	27
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	**	19	23
Fairchild Semiconductor					DATA I/O Part Number											
	1024x8 MOS	24	2708	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**	21	27
Fujitsu					DATA I/O Part Numbers											
	1024x8 MOS	24	8518 (2708)	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**	21	27
	2048x8 MOS	24	8516 (2716)	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	**	19	23
	4096x8 MOS	24	8532 (2732A)	VOL TS	1512	A	1620	A	D	0075	E	1576	1705	**	27	24
	4096x8 MOS	24	8532 (2732)	VOL TS	1512	C	1531	E	D	0075	E	1572	1705	**	19	24
	8192x8 MOS	28	2764	VOL TS	1512	A	1622-001	F	E	0074	A	1564-001	0042	**	35	33
	8192x8 MOS	28	27C64	VOL TS	1512	A	1622-001	F	E	0074	A	1564-001	0042	**	35	33
General Instruments					DATA I/O Part Numbers											
	2048x8 MOS	24	5716 (EEPROM)	VOL TS	-	-	-	-	-003	-002	-	-	-	-	83	23
Harris Semiconductor					DATA I/O Part Numbers											
	256x4 CMOS	16	6611R	VOL TS	1319-3	E	1345-2	-	-	-	-	-	-	-	23	
	256x4 CMOS	16	6661	VOL TS	1319-3	E	1399-2	-	-	-	-	-	-	-	23	
	512x8 CMOS	24	6641	VOH TS	1777-001	A	1776-001	F	-	-	-	-	-	40	47	
	512x8 CMOS	24	6616	VOH TS	1777-001	A	**	**	**	-	-	-	-	**	**	
Hitachi					DATA I/O Part Numbers											
	2048x8 MOS	24	48016 (EEPROM)	VOL TS	1512	A	1510	F	A	**	**	**	**	**	34	23
	2048x8 MOS	24	462716	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	**	19	23
	4096x8 MOS	24	482732A	VOL TS	1512	A	1620	A	D	0075	E	1576	1705	**	27	24
	4096x8 MOS	24	462532	VOL TS	1512	A	1511	E	C	0075	A	1571	1359-2	**	19	25
	4096x8 MOS	24	482732	VOL TS	1512	A	1531	A	D	0075	A	1572	1705	**	19	25
	8192x8 MOS	28	482764	VOL TS	1512	A	1622-001	F	E	0074	A	1564-001	0042	**	35	33
Intel					DATA I/O Part Numbers											
	256x8 MOS	24	1702A/4702A/8702A	VOH TS	1183-1	C	1047	-	-	-	-	-	-			
	512x8 MOS	24	2704/8704	VOL TS	1174-1	G	1033-2	A	A	0075	A	1567	1359-1	A	21	26
	1024x8 MOS	24	2708/8708	VOL TS	1174-1	F	1033-4	A	A	0075	A	1566	1359-1	A	21	27
	1024x8 MOS	24	2758	VOL TS	1512	A	1366-4	A	A	0075	A	1570	1359-2	A	19	22
	1024x8 MOS	40	2758 S1865	VOL TS	1512	A	1366-3	A	A	-	-	-	-	-	19	35
	1024x8 MOS	40	8741/8748A	VOH TS	1417	A	1448	-	-	0073-001		1860-001		-	-	-
	2048x8 MOS	40	8749H	VOH TS	1417	A	**	-	-	0073-001		1860-003	-	-	-	-
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	A	19	23
	2048x8 MOS	24	2816 (EEPROM)	VOL TS	-	-	-	H	-002	-	-	-	-	A	37	23
	2048x8 MOS	40	8755	VOH TS	1417	A	1447-1	-	-	-	-	-	-	-	-	-
	2048x8 MOS	40	8755A	VOH TS	1417	A	1447-2	-	-	0073-001		1861-001	-	-	-	-
	2048x8 MOS	24	2815 (EEPROM)	VOL TS	-	-	-	-003	-002	-	-	-	-	**	85	23
	4096x8 MOS	40	8751	VOL TS	1512	C	**	-	-	-	-	-	-	-	-	-
	4096x8 MOS	24	2732	VOL TS	1512	C	1531	A	D	0075	F	1572	1705	A	19	24
	4096x8 MOS	24	2732A	VOL TS	1512	A	1620	A	D	0075	E	1676	1705	A	27	24
	8192x8 MOS	28	2764	VOL TS	1512	A	1622-001	-003	-002	0074	A	1564-001	0042	A	79	33
	16384x8 MOS	28	27128	VOL TS	-	-	-	-002	-002	**	-	**	-	A	35	51
Intersil					DATA I/O Part Numbers											
	512x8 CMOS	24	6854	VOL TS	1416-1	E	1450	-	-	-	-	-	-			
	1024x8 CMOS	24	6658	VOL TS	1416-1	E	1706-001	-	-	-	-	-	-			
	1024x4 CMOS	24	6663	VOL TS	1416-1	E	1449	-	-	-	-	-	-			
	2048x4 CMOS	24	6657	VOL TS	1416-1	E	1707-001	-	-	-	-	-	-			
Mitsubishi					DATA I/O Part Numbers											
	256x8 MOS	24	58563S(1702A)	VOH TS	1183-1	C	1047	-	-	-	-	-	-			
	1024x8 MOS	24	58732S(2708)	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**	21	27
	1024x8 MOS	24	2708	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**	21	27
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	**	19	23
	4096x8 MOS	24	2732	VOL TS	1512	A	1531	A	F	0075	A	1572	1705	**	19	24
	8192x8 MOS	28	2764	VOL TS	**	-	**	**	**	**	**	**	**	**	**	**
Mostek					DATA I/O Part Numbers											
	256x8 MOS	24	3702	VOH TS	1183-1	C	1047	-	-	-	-	-	-			
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	A	A	0075	A	1569	1359-2	**	19	23
Motorola					DATA I/O Part Numbers											
	1024x8 MOS	24	MCM68708/2708	VOL TS	1174-1	G	1033-4	A	A	0075	A	1566	1359-1	**		
	1024x8 MOS	28	MCM2808 (EEPROM)	VOL TS	-	-	-	-003	-002	-	-	-	-	-	82	72
	2048x8 MOS	24	TMS2716	VOL TS	1174-1	H	1398	A	A	0075	A	1568	1405-1	**	23	28
	2048x8 MOS	24	MCM2716	VOL TS	1512	A	1710	B	A	0075	E	1569	1359-2	**	19	23
	2048x8 MOS	40	MCM68701	VOL TS	0035-001	-	0036-001	-	-	-	-	-	-	-	-	-
	2048x8 MOS	28	MCM2817 (EEPROM)	VOL TS	-	-	-	-003	-002	-	-	-	-	-	81	71
	2048x8 MOS	24	MCM2816 (EEPROM)	VOL TS	-	-	-	-003	-002	-	-	-	-	-	43	23
	2048x8 MOS	24	MCM2815 (EEPROM)	VOL TS	-	-	-	**	**	-	-	-	-	-	**	**
	4096x8 MOS	24	MCM68732-0	VOL TS	-	-	-	F	E	0075	F	1713 (4)	-	-	25	44
	4096x8 MOS	24	MCM68732-I	VOL TS	-	-	-	F	E	0075	F	1713 (4)	-	-	25	45
	4096x8 MOS	24	MCM2532	VOL TS	1512	A	1711	B	A	0075	E	1713	1359-2	-	19	25
	4096x8 MOS	28	MCM2832 (EEPROM)	VOL TS	-	-	-	-003	-002	-	-	-	-	-	81	70
	8192x8 MOS	24	MCM68764 / 68766	VOL TS	-	-	-	F	E	0075	F	1574 (4)	**	-	25	29

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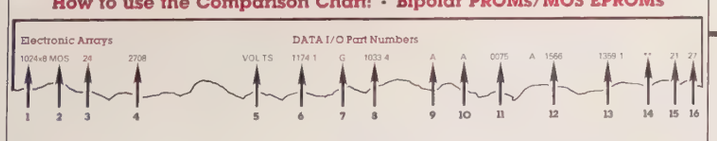
Array	Technology	Pinout	Device	Logic Level	Card Set	Rev.	Socket Adapter	Unipak	Family	Pinout
National Semiconductor					DATA I/O Part Numbers					
	256x8 MOS	24	4203/5203	VOL TS	1178-1	B	1047	-		
	256x8 MOS	24	1702A	VOH TS	1183-1	C	1047	-		
	512x8 MOS	24	4204 5204	VOH TS	1177-1	H	1033	-		
	1024x8 MOS	24	2708	VOL TS	1174-1	G	1033-4	A		
	1024x8 MOS	24	2758A	VOL TS	1512	A	1366-4	A		
	1024x8 MOS	24	2758B	VOL TS	1512	A	1366-3	A		
	2048x8 MOS	24	2816 (EEPROM)	VOL TS	-	-	-	-003		
	2048x8 MOS	24	9716 (EEPROM)	VOL TS	-	-	-	-003		
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	A		
	2048x8 CMOS	24	27C16	VOL TS	1512	A	1710	E		
	2048x8 CMOS	24	6716	VOL TS	-	-	-	**		
	4096x8 MOS	24	2532	VOL TS	1512	A	1511	A		
	4096x8 MOS	24	2732	VOL TS	1512	A	1531	A		
Nippon Electric Co., Ltd.					DATA I/O Part Numbers					
	256x8 MOS	24	D454D	VOH TS	1269-1	A	1031-1	-		
	1024x8 MOS	28	D458D	VOH TS	1269-1	A	1130	-		
	1024x8 MOS	40	8741/8748	VOH TS	**	-	**	-		
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	F		
	2048x8 MOS	40	8755A	VOH TS	**	-	**	-		
	4096x8 MOS	24	2732	VOL TS	1512	A	1531	F		
Oki					DATA I/O Part Numbers					
	1024x8 MOS	24	2708	VOL TS	1174	A	1033-4	A		
	1024x8 MOS	24	2758	VOL TS	1512	A	1366-4	A		
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	A		
	2048x8 MOS	40	8755A	VOH TS	1417	A	1447-2	-		
RCA					DATA I/O Part Numbers					
	256x8 CMOS	24	18U42	VOH TS	1374	A	1621	-		
Signetics					DATA I/O Part Numbers					
	1024x8 MOS	24	2708	VOL TS	1174-1	G	1033-4	A		
Synertek					DATA I/O Part Numbers					
	2048x8 MOS	24	2716	VOL TS	1512	A	1510	**		
Texas Instruments					DATA I/O Part Numbers					
	1024x8 MOS	24	2508	VOL TS	1512	A	1366-4	A		
	1024x8 MOS	24	2708/27L08	VOL TS	1Y4-1	H	1033-4	A		
	2048x8 MOS	24	2716	VOL TS	1174-1	H	1398	A		
	2048x8 MOS	24	2516	VOL TS	1512	A	1510	A		
	4096x8 MOS	24	2532	VOL TS	1512	A	1511	D		
	8192x8 MOS	28	2564	VOL TS	1512	A	1936	G		
Toshiba					DATA I/O Part Numbers					
	512x8 MOS	24	321 (2704)	VOL TS	1174-1	T	1033-2	A		
	1024x8 MOS	24	322 (2708)	VOL TS	1174-1	T	1033-4	A		
	2048x8 MOS	24	323 (27161V)	VOL TS	1512	A	1510	A		
	2048x8 MOS	40	8756AC	VOH TS	1417	A	1447-2	-		
	4096x8 MOS	24	2732	VOL TS	1512	A	1531	A		

How to use the Comparison Chart: - Bipolar PROMs/MOS EPROMs



1. **Array Size —** PROMs bit storage capacity (e.g., 2048 words x 8 bit word)
2. **Technology —** PROMs method of construction
   FL = Fusible Link
   MOS - Metal Oxide Semiconductor
   CMOS - Complementary Metal Oxide Semiconductor
   AIM = Avalanche Induced Migration
   ECL - Emitter Coupled Logic
   DEAP - Diffused Eutectic Aluminum Process
   ISOZ - ISO Planer Z
3. **Pinout —** Indicates the number of pins of the device leadframe (e.g. 24)
4. **Device Designation —** The device designation represents the manufacturer's designation. Multiple entries on the same line have identical programming requirements, but different operation or part numbering. Refer to manufacturer's literature for more specific information.
   † = Part no longer in production. Check with manufacturer for availability
5. **Logic Level —** VOL = Blank PROM contains logical "1". Selectively programmed to logical "0"
   VOH = Blank PROM contains logical "0". Selectively programmed to logical "1"
   OC = Open Collector
   TS = Tri State
   OE = Open Emitter
6. **Programming Module (909/919-XXXX) —** Programming Paks for System 19 and System 17 (e.g., 919-1512)
   Program Card Sets for Models 1, 2, 3, 5, 7, 9 (e.g., 909-1512)
   Interchangeable programming modules have been tested to meet rigid vendor specifications, and have been approved in writing by the semiconductor manufacturers
   ** = Under development
7. **Revision Level —** The revision level specifies the earliest version of the programming module that will program the PROM to its manufacturer's latest programming specifications. All later revision programming modules may be used as well. Older programming modules can generally be updated to new specifications in the field through modification and/or recalibration. Contact a Data I/O Service Center for update information.
8. **Socket Adapters (715-XXXX) —** Socket adapters match programming module outputs to device pinout, word limit and byte size requirements (e.g., 715-1510) For Flat Pak socket adapters contact your Data I/O representative. Note, some early model Data I/O programmers may require retrofit of a 709-1012 shielded interface cable between the programming module and socket adapter. Contact a Data I/O Service Center if assistance is needed in cable identification.
9. **UniPak (950-0099) Revision Level —** UniPak for System 19 and System 17 programs all popular N-Channel MOS EPROMs and most popular Bipolar Generic PROM families. The letter in this column gives the earliest revision of the UniPak which will program the PROM to its manufacturer's latest programming specifications. All later revision UniPaks may be used as well. The absence of a letter means the part can not be programmed using the UniPak
10. **MOS Pak (950-0076) Revision Level —** MOS Pak for System 19 and System 17 programs all popular N-Channel MOS EPROMs. The letter in this column gives the earliest revision of the MOS Pak which will program the PROM to its manufacturer's latest programming specifications. All later revision MOS Paks may be used as well. The absence of a letter means the part cannot be programmed using the MOS Pak
11. **Gang Module (950-XXXX)/Revision Level —** Gang Module for System 19 and System 17 programs the device indicated eight at a time. Must be used with appropriate characterizer. Consult your Data I/O representative for part numbers and software modifications which may be required. The revision level letter gives the earliest revision of the Gang Module which will program the PROM to its manufacturer's latest programming specifications. All later revision Gang Modules may be used as well. The absence of a letter means the part cannot be programmed using the Gang Module.
12. **Characterizer (714-XXXX) —** Characterizer for Gang Module matches Programming Electronics to the device type (e.g., 714-1569)
13. **Gang Socket Adapter (715-XXXX) - Model 16 —** The socket adapter matches programming electronics output to device pinout, word limit, and byte size requirements (e.g., 715-1359-2) With the Gang Socket Adapter, the Model 16 programs the device indicated sixteen at a time.
14. **Model 120/121** - The Model 120 programs all major MOS EPROMs 20 at a time. The Model 121 has the same capabilities as the Model 120 with the increased benefit of being able to program sets
15. **Family Code** - Family Code for all software selectable modules.
16. **Pinout Code** - Pinout Code for all software selectable modules.

** = Under development
† = Part no longer in production

BIPOLAR PROMS

Array	Technology	Pinout	Device	Logic Level	Card Set	Rev.	Socket Adapter	Unipak	Family	Pinout
Advanced Micro Devices					DATA I/O Part Numbers					
	32x8 FL	16	27S18/29750A	VOH OC	1286-1	G	1407-1	A	16	02
	32x8 FL	16	27S19/29751A	VOH TS	1286-1	G	1407-1	A	16	02
	256x4 FL	16	27S20/29760A	VOH OC	1286-1	G	1408-1	A	16	01
	256x4 FL	16	27S21/29761A	VOH TS	1286-1	G	1408-1	A	16	01
	512x4 FL	16	27S12 29770	VOH OC	1286-1	G	1408-2	A	16	03
	512x4 FL	16	27S13/29771	VOH TS	1286-1	G	1408-2	A	16	03
	512x8 FL	24	27S15	VOH TS	1286-1	G	1411-1 (1)	-		
	512x8 FL	24	27S24/25	VOH OC/TS	1286-1	G	1617	-003	82	66
	512x8 FL	22	27S26/29774	VOH OC	1286-1	G	1412-2	-		
	512x8 FL	22	27S27/29776	VOH TS	1286-1	G	1412-2	-		
	512x8 FL	20	27S28/29	VOH OC/TS	1286-1	G	1413	E	16	09
	512x8 FL	24	27S30/31	VOH OC/TS	1286-1	G	1545	A	16	36
	1024x4 FL	18	27S32/33	VOH OC/TS	1286-1	G	1414	E	16	38
	1024x8 FL	24	27S35/37	VOH TS	1286-1	G	1723	-003	62	66
	1024x8 FL	24	27S180/181	VOH OC/TS	1286-1	G	1548-2	A	16	37
	1024x8 FL	24	27S280/281	VOH OC/TS	1286-1	G	**	-003	16	37
	2048x4 FL	18	27S184/185	VOH OC/TS	1286-1	H	1816	E	16	06
	2048x8 FL	24	27S45/47	VOH TS	1286-1	J	1660-001	-		
	2048x8 FL	24	27S190/191	VOH OC/TS	1286-1	H	1688-1	H	16	68
	2048x8 FL	24	27S290/291	VOH OC/TS	1286-1	H	1888-2	-003	16	68
	4096x4 FL	20	27S40/41	VOH OC/TS	1286-1	H	1282	-		

(1) Rev. D required for Rev. H and above programming modules

Array	Technology	Pinout	Device	Logic Level	Card Set	Rev.	Socket Adapter	Unipak	Family	Pinout
Fairchild Semiconductor					DATA I/O Part Numbers					
	256x4 FL	16	93417/427	VOL OC/TS	1063-2	H	1035-1	A	01	01
	256x4 ECL	16	10416/100416	VOL OE	1507	A	1003-4	-		
	256x4 ECL	16	10459/100459	VOL OE	**	**	**	-		
	512x4 FL	16	93436/446	VOL OC/TS	1063-2	H	1035-2	A	01	03
	512x8 FL	24	93438/448	VOL OC/TS	1063-2	H	1033-2	A	01	15
	1024x4 FL	18	93452/453	VOL OC/TS	1063-2	H	1039-3	A	01	05
	1024x8 FL	24	93450/450	VOL OC	1063-2	H	1033-3	A	01	16
	1024x8 FL	24	93451/451	VOL TS	1063-2	H	1033-3	A	01	16
	1024x8 FL	24	93460/461	VOL OC/TS	1063-2	H	1033-3	A	01	16
	1024x8 ISOZ	24	93Z450/451	VOH OC/TS	0043-001	A	1722-001	-		
	2048x8 ISOZ	24	93Z510/511	VOH OC/TS	0043-001	A	1722-002	-		
	8192x8 ISOZ	24	93564/565	VOH OC/TS	0043-001	A	1722-003	-		
	4096x4 ISOZ	24	93612/513	VOH OC/TS	0043-001	A	**	-		
Fujitsu					DATA I/O Part Numbers					
	32x8 DEAP	16	7056/51	VOH OC/TS	1268-1	A	1302-1	-		
	256x4 DEAP	18	7057/52	VOH OC/TS	1268-1	A	1303-1	-		
	512x4 DEAP	18	7058/53	VOH OC/TS	1268-1	A	1303-2	-		
	1024x4 DEAP	18	7059/54	VOH OC/TS	1268-1	A	1305-5	-		
	1024x8 DEAP	24	7060/56	VOH OC/TS	1268-1	A	1455	-		
	256x8 DEAP	24	7119/20	VOH OC/TS	1488	A	1558	-		
	512x8 DEAP	20	7123/24	VOH OC/TS	1488	A	1559	-		
	1024x4 DEAP	18	7121/22	VOH OC/TS	1488	A	1305-5	-		
	1024x8 DEAP	22	7129/30	VOH OC/TS	1488	A	0075-002	-		
	1024x8 DEAP	24	7131/32	VOH OC/TS	1488	A	1618-1	-		
	2048x8 DEAP	18	7127/28	VOH OC/TS	1488	A	1619	-		
	2048x8 DEAP	22	7135/36	VOH OC/TS	1488	A	0075-001	-		
	2048x8 DEAP	24	7137/38	VOH OC/TS	1488	A	1618-2	-		
	4096x4 DEAP	20	7133/34	VOH OC/TS	1488	A	0076-001	-		
	4096x8 DEAP	24	7141/42	VOH OC/TS	1488	A	0077-001	-		
Harris Semiconductor					DATA I/O Part Numbers					
	32x8 FL	16	7602/03	VOL OC/TS	1473-002	A	1037	A	05	02
	64x8 FL	24	6612	VOH OC	1064-3	H	1033	-	-	-
	256x4 FL	16	7610/11	VOL OC/TS	1473-002	A	1035-1	A	05	01
	512x4 FL	16	7620/21	VOL OC/TS	1473-002	A	1035-2	A	05	03
	512x8 FL	24	7640/41	VOL OC/TS	1473-002	A	1680-003	A	05	15
	512x8 FL	24	7646R1	VOL OC	1063-4	G	1411-2(3)	-		
	512x8 FL	24	7647R	VOL TS	1473-002	A	1671 001	-		
	512x8 FL	20	7648/49	VOL OC/TS	1473-002	A	1558	A	05	09
	1024x4 FL	18	7642/43	VOL OC/TS	1473-002	A	1039-3	A	05	05
	1024x4 FL	16	7644/1	VOL OC	1063-4	G	1042	A	05	04
	1024x4 FL	18	7643P	VOL TS	1473-002	A	1039-3	E	05	38
	1024x8 FL	24	7608†	VOL TS	1063-4	G	1628-1	A	05	16
	1024x8 FL	24	7680/81	VOL OC/TS	1473-002	A	1680-002	A	05	16
	1024x8 FL	24	7681P	VOL TS	1473-002	A	1680-002	A	05	16
	2048x4 FL	18	7684/85	VOL OC/TS	1473-002	A	1718-001	A	05	06
	2048x4 FL	18	7685P	VOL TS	1473-002	A	1718-001	A	05	06
	2048x4 FL	20	7686/87†	VOL OC/TS	1063-4	P	1394	A	05	10
	2048x8 FL	24	7616D1	VOL OC	1063-4	P	1628-2	A	05	21
	2048x8 FL	24	76161	VOL TS	1473-002	A	1680-001	A	05	21
	2048x8 FL	24	7616	VOL TS	1473-002	A	1680-004	A	05	42
	4096x4 FL	20	76165	VOL TS	1473-002	A	1720-001	-		
	4096x8 FL	24	76321	VOL TS	1473-002	A	1698-001	H	05	63
	8192x8 FL	24	76641	VOL TS	-	-	-	H	05	67

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Array	Technology	Pinout	Device	Logic Level	Card Set	Rev.	Socket Adapter	Unipak	Family	Pinout
Hitachi					DATA I/O Part Numbers					
	1024x4 AIM	18	25044 45	VOH OC/TS	1550	A	1305-5	-		
	1024x8 AIM	24	25088/89	VOH OC/TS	1550	A	1618-1	-		
	2048x4 AIM	18	25084/85	VOH OC/TS	1550	A	1618	-		
	2048x8 AIM	24	25168/69	VOH OC/TS	1550	A	1618-2	-		
Intel					DATA I/O Part Numbers					
	1024x8 FL	24	3608†	VOL OC	0042-001	A	1709-002	-		
	1024x8 FL	24	3628 3628A	VOL TS	0042-001	A	1709-002	-		
	1024x8 FL	24	82S/HS181	VOL TS	0042-001	A	1709-002	-		
	2048x8 FL	24	36161	VOL OC	0042 001	A	1709-001	-		
	2048x8 FL	24	3636-3636B	VOL TS	0042-001	A	1709-001	-		
	2048x8 FL	24	82S/HS191	VOL TS	0042-001	A	1709-001	-		
	4096x8 FL	24	3632	VOL TS	0042-001	A	1628-2	-		
	4096x8 FL	24	82S/HS321	VOL TS	0042-001	A	1628-2	-		
Intersil					DATA I/O Part Numbers					
	32x8 AIM	16	5600/10	VOH OC/TS	1268-1	A	1302-1	-		
	256x4 AIM	16	5603A/23	VOH OC/TS	1268-1	A	1303-1	-		
	512x4 AIM	16	5604/24	VOH OC/TS	1268-1	A	1303-2	-		
Monolithic Memories					DATA I/O Part Numbers					
	32x8 FL	16	5330/6330	VOL OC	1226-1	M	1046	A	29	02
	32x8 FL	16	5331/6331	VOL TS	1226-1	M	1046	A	29	02
	256x4 FL	16	5300/6300	VOL OC	1226-1	M	1035-1	D	11	01
	256x4 FL	16	5301/6301	VOL TS	1226-1	M	1035-1	D	11	01
	256x8 FL	24	5335 6335	VOL OC	1226-1	M	1033-1	D	11	14
	256x8 FL	24	5336 6336	VOL TS	1226-1	M	1033-1	D	11	14
	256x8 FL	20	5308 6308	VOL OC	1226-1	M	1028-1	D	11	08
	256x8 FL	20	5309 6309	VOL TS	1226-1	M	1028-1	D	11	08
	512x4 FL	16	5305 6305	VOL OC	1226-1	M	1035-2	D	11	03
	512x4 FL	16	5306 6306	VOL TS	1226-1	M	1035-2	D	11	03
	512x8 FL	24	5340 6340	VOL OC	1226-1	M	1033-2	D	11	05
	512x8 FL	24	5341/6341	VOL TS	1226-1	M	1033-2	D	11	05
	512x8 FL	24	5340JS 6340JS	VOL OC	1226-1	M	1623-004	D(1)	11	05
	512x8 FL	24	5341JS 6341JS	VOL TS	1226-1	M	1623-004	D(1)	11	05
	512x8 FL	20	5348 6348	VOL OC	1226-1	M	1559	D	11	09
	512x8 FL	20	5349/6349	VOL TS	1226-1	M	1559	D	11	09
	1024x4 FL	18	5350 6350	VOL OC	1226-1	M	1036	-		
	1024x4 FL	18	5351 6351	VOL TS	1226-1	M	1036	-		
	1024x4 FL	18	5352 6352	VOL OC	1226-1	M	1039-3	D	11	05
	1024x4 FL	18	5353/6353	VOL TS	1226-1	M	1039-3	D	11	05
	1024x8 FL	24	5380/6380	VOL OC	1226-1	M	1033 3	D	11	16
	1024x8 FL	24	5381/6381	VOL TS	1226-1	M	1033-3	D	11	16
	1024x8 FL	24	5380JS/6380JS	VOL OC	1226-1	M	1623-007	D(1)	11	05
	1024x8 FL	24	5381JS 6381JS	VOL TS	1226-1	M	1623-007	D(1)	11

devices which are quad two line to one line converters. They gate the data in through the Selector and into Complement gates which are used to invert the data by use of the switch S1. Data are then presented to the Data Read Out gates U9 and U16 to present the data from that point on to the DO Buss at the upper right hand corner of the drawing. The data is gated on the Buss at Read time, when Pin P at the input connector becomes high. During that period, data is stable, and the Reader is not advanced until after the Read Pulse occurs, and then Address, at which time the Reader moves to the next character position. The Selector gates U7, and U6, are selected by the input device Pin F being ground, the Reader Enable line Pin K, being open, and the Remote Interface line Remote Select, being in a False condition.

2.4.2.4 REMOTE INPUT

Remote Input occurs when Pin 18 of connector J1 is brought to ground. All Remote Input lines are pulled up to +12 Volts with low pass filter networks composed of a capacitor to ground and a resistor to +12, filtering out any extraneous noises that may occur on the input interface. All input line receivers have a 5 Volt threshhold and are 339 type devices for the level detection. As the Remote Interface is selected, the output of the Selector, U3 Pin 1, becoming ground, turns off Inverter, U10 Pin 6, so that it becomes high, thereby selecting the Remote Interface instead of Reader. The Select line, becoming high, is also presented as a high level to the Strobe Memory, U12 Pin 2 and Pin 13, as well as the Input Ready Gate, U18 Pin 12, and the clamp release on Data Memory U19 Pin 10. These lines becoming high, condition the System to accept remote input data and allows the Input Ready Gate to become true, thereby driving the Ready/Busy Interface (Pin N) to ground signifying Buss busy. The System will remain in a wait state until the arrival of Data along with the first Strobe, Pin 9 of J1. All Data Lines and Strobe pass through low pass filter and level detection gates. The output of the Strobe Gate, U3 Pin 13, located in the center of the drawing, sets the Strobe Memory on the leading edge of the pulse. The Strobe Memory sets U12 Pin 8 to ground, thereby releasing the Busy clamp on the Control Buss and allowing the Control System to proceed to issue Read, and take the data from the Input Interface and store it in the Control Card. As soon as the Address has been issued signifying the completion of the signal, the Strobe Memory is again cleared, thereby driving the Buss Busy, once again awaiting the arrival of the next remote input Character and Strobe.

To emulate a BRPE Perforator, whenever the select for output is enabled, the Perforator Sync Clock, U5, is turned on and allowed to be present to Pin 12 of the Remote Interface. This Clock is simply used to signal the Remote Interface that Data I/O Programmers are ready for input data. A Busy Ready signal is applied to Pin 15 of the Interface with Pin 16 signifying End of Data, so that a complete handshake of information and interlock of Busy occurs at the interface. All lines are of a high level nature for maximum noise immunity. Plus 12 volts is applied to Pin 14 of connector J1 so that the end user at the Computer Interface may utilize this level to power high noise immunity drivers as required.

As Word Limit is reached on the Data Buss Interface of the Programmer, the Word Limit sets the End Data Memory, which drives the End Data line to ground signaling the Interface that no more input is possible of being accepted. This Memory will remain in the Set condition until Reset occurs.

2.5 RAM BUFFER

The Model 5 RAM is a standard 4K x 8. Refer to drawing 008-1433. Input Address is located in the upper left hand corner of the drawing labeled A0 through A11 and are applied through Isolation 7407 Buffer devices, U20 and U24. These Address Lines are applied in parallel to all RAM's simultaneously with the A10 line being used as the Chip Enable for either the left hand row or right hand row of RAM's depending on the level of A11.

The eight data lines arriving on Pin M through V are applied through 7405 buffer amplifiers U19 and U23, which are also applied to both rows of RAM's, with the one bit being applied to U1 and U2, the two bit applied to U3 and U4, the three bit applied to U5 and U6, and so forth down the card. With all RAM's installed, an eight bit word may be written into any location from Ø to 4095 locations or retrieved from the RAM through the Data Output Gates and presented to the DO Buss located on the right hand side of the drawing.

2.5.1 SELECTION OF MODE

Two lines are used to determine selection of mode namely Write (PP) and Read (RR). In order to write data into the RAM Buffer, the Write Inhibit Line (PP) must be driven to ground and Data and Address must be applied to the System. When all of these requirements are stable, the Write pulse Pin AA is driven low for the normal Clock period which turns on the Read Write line Pin 3 of all RAM devices. The Data and Address selects the row, Address, and Data Inputs to all of the proper RAM's so that when the Read Write line is driven low, the data is stored in that location. The stored data is presented through the Data Output Gates at all times except during a Read cycle when Pin X occurs. This occurs because as the Write Inhibit Line PP is Driven to ground, Inverter U21 Pin 4 enables the Write R Read Out Gate U22 Pin 13. When the Address line Pin 24 is ground, and the Read Pulse is not there on Pin X, the Address Read Out gate, U21 Pin 13, enables the Write Read Out gate U22 Pin 12, thereby allowing the data from the RAM's to be applied through the Data Read Out Gates onto the DO Buss for display.

2.5.2 READING DATA FROM RAM

If the Read Inhibit Line RR is driven low, and the Read pulse Pin X is allowed to become high, during the time of Read, the Read Select Gate U22 Pin 6 becomes low, thereby enabling the Data Output Gates at the Address occation defined, which puts the data from the RAM onto the DO Buss for storage into the Control Card. Eight and four bit levels are selectable by the two jumpers 8 Bit/4 Bit for both data output control and high order low order display for Pin 19 and W located on the right hand side of the drawing.

If 1Kx4 RAM's are to be installed in the System, the basic RAM then includes U1, U3, U5, and U7. All other RAM Buffers are removed from the System as they are not required. If 1Kx8 devices are to be installed, then the first row of RAMS U1, U3, U5, U7, U8, U10, U12, and U15, are installed. This also allows 8 Bits of data to be presented to the Output Buss as soon as the 8 Bit jumpers have been put in the proper place in the card.

4K x 4 configuration allows U1 through U6, U7, and U14 to be inserted with the rest of the RAM's being left off. The 4 Bit jumpers must be in place and at that time the System will function as a 4K x 4 RAM.

With all RAM's in place and the 8 Bit jumpers in place, the System functions with a 4K x 8 RAM Buffer.

2.6 ADDRESS CARD

The Address Card, Drawing No. 008-1431, is a card containing the Address Counter for controlling the positioning pointer for all address locations in the control system. It also contains a binary to BCD Converter, and Direction Memory and Word Limit control. Referring to the drawing at the end of the manual, the Address Counter, consisting of devices U4, U3 and U9 (74193 counters) have for Inputs, a Forward and Reverse Gate for counting up or counting down. The Direction control occurs form the Direction Memory U17 Pin 5. For manual operation, the Forward and Reverse keys enter the card on Pin 28 and FF, which are presented through 8094 devices, gated with the Forward and Reverse Test pulse from the control card (Pin H).

The Direction Memory is presented into the Model III Direction Gate, U5 Pin 13, which is enabled when the Jumper JP1 is removed. This Jumper also allows the Model III Advance Gate, U16 Pin 6, to be enabled and disables the normal gate, U16 Pin 3, (which is used for Model I and II applications). Pin F, inbound, is the Increment Address line, which is controlled from the Control Card on a separate line from Input Increment for controlling the Reader or other input devices. The Directional Control Gate, U5 Pin 11, is therefore applied to Pin 20 to exit to the rest of the Bus Control System for Directional control. This line is also applied to the Forward and Reverse gates, U5 Pin 2, and U5 Pin 5, via inverter U10 and 12. The Increment Address pulse, arriving on Pin F, is therefore applied through the Model III gate, U16 Pin 6, to test both Forward and Reverse gates, U5 Pin 1 and 4. The Direction Memory therefore controls the countup or countdown function of the Address Counter.

2.7 ADDRESS BUFFERS

The Address Counter is presented through 7407 devices, U14 and U15, which are from that point presented to the Bus System, to drive all Address lines in the Programmer. The purpose of the 7407s are isolation amplifiers and drivers so that no bus short or level loading may effect the Address Counter.

2.8 BINARY TO BCD CONVERSION

The Address Counter is also applied to the 74185 devices for binary to BCD conversion. These devices are arranged in such a manner so as to provide a four decimal output display with input lines A_0 through A_{11}. The output of the 74185 devices are applied on the right-hand side of the drawing directly to the front panel display to the three or four digit Word Count. They drive directly the HP7300 decimal display devices.

2.9 WORD LIMIT

As the Address Counter is proceeding through the Word Count, and Word Limit occurs, as is controlled by the Program Card set inserted into the system, Pin CC, located in the lower left-hand corner of the drawing would be driven low. This line gates the input to the Word Limit Memory, U17 Pin 12, whose test line arrives from the Input Busy test pulse Pin 21. As U17 Pin 8 becomes high on the leading edge of the Input Busy test pulse, the Direction Memory is reversed by clocking the input U17 Pin 3 of the Direction Memory, which serves as a divide by two binary. This will cause the direction of the system to be reversed so that the opposite mode of operation for direction is selected by the Model III bus structure.

2.10 LIMIT ZERO

The Address Counter "carry" output (U9 Pin 12), is utilized for limit zero control. When the Reverse Counter is counting down and decrements past zero to maximum Word Count, and the Direction Memory at that time is reversed, the first count pulse will cause a CARRY pulse from U9 Pin 12, which is presented to the control card as Limit Zero. This line is used to shift modes from BLANK CHECK to PROGRAM followed by VERIFY and then STOP in the AUTOMATIC mode of operation. This line is not used in the MANUAL mode of operation.

2.11 HEXIDECIMAL TRANSLATOR

The Hexidecimal option for the Model V series Instruments allows data to be entered from a Hexidecimal Front Panel Mounted Pad for data preparation in either true or complement form. This option allows receipt of data from an input device in ASCII and converts that data to Hexidecimal onto the output device, which will be RAM Buffer. Normal conversion from an input device to RAM is accomplished by subroutine jump software in to Control Card.

A two digit display (Hex) or three digit display (Octal) accompanies the pad on the System for data input and bus operation display. When preparing information into the Programmer from the pad, each Keystroke shall clear the data which was resident in the Control Card Data Register and uptdate that data with the entered word. The Entry System causes a shift and then load subroutine to be accomplished into the Resident Data Output Register on the Translator Card, which, when the cycle has been completed interrogates the Control Card for updating of its Data Register. The display, therefore, is a result and echo of the transition from Keyboard prepared data to store information in the Control Card Data Buffer.

Data may be entered from the Keyboard in either its true form or complement form which is selected by a Data Invert Switch, located on the Translator Card. The data inversion is very useful when programming some PROMs which program VOH instead of VOL and in that method, a complement form of data must be resident in the Programmer in order to properly program the inverted type of PROMs. The ASCII Hex Translator is optionally convertible to Octal with two Jumpers on the Card. The Jumpers convert the data so that a three Bit input word instead of four is excepted from a Keyboard and a three digit or position shifting prior to load is accomplished in the Hex operation. Two PROMs are located on the Converter Card to receive input ASCII data from the remote device such as Paper Tape Reader, computer of other specified device and converts that data to Hexidecimal (or Octal) with sub-routine control to determine start of message, stopping, or end of program word.

Referring to the appropiate pad, Octal or Hexidecimal at the end of the manual Drawing No. 1091 (Hex) and 1092 (Octal), the input data switches are presented into a diode module encoder HM1-013. Associated with the Hexidecimal Card is a two digit display using HP7340 type devices to accommodate the 16 Bit input data word for zero through F. The two displays, therefore, in their FF condition, display 8 Bits of information. The program for the diode modules are identical and are located in the upper right hand corner of each drawing. It can be seen on the Hexidecimal Input Keyboard that switches Ø through 7 are presented to the UI diode encoder and switches 8 through F are presented to the

U2 diode encoder. Zero and 8 are identical with the exception of Bit 5 which encodes an 8 Bit for each Keyswitch depressed in switches 8 through F. Each key then presents an integer input of +5 volts into the encoder whose output is a common or'ed clock line with binary Bits 1, 2, 4, 8 being applied to the external connector J.3. In addition to the data switches, WORD CLEAR, ADD FORWARD, and ADD REVERSE switches are utilized on the Hexidecimal pad with returning display of the High and Low order bytes for the 7340 devices.

The Octal Keyboard, Drawing 1092, is very similar to the Hexidecimal device with the exception that it has 7300 type displays and a single diode module encoder. The code program for the diode module is identical to Hexidecimal and is also located on the 1092 Drawing. Eight switches are located for data at the left hand side of the Drawing which input to the single diode module to encode a three Bit (1, 2, 4) code format with or'ed clock in identically the same manner as did Hexidecimal. The other switches assiciated with the Octal pad are WORD CLEAR. ADD FORWARD, ADD REVERSE, and ENTER. The ADD FORWARD and ADD REVERSE keys are used for data slewing in normal system operation whereas the ENTER key, located below the data keys, is used for entry into the system, the data which was prepared. It is the same as SPACE BAR on the Binary Keyboard. The returning data for display is accomplished with a maximum display of 777 to accomodate eight Bits of information.

2.11.1 TIMING

Referring to the Timing Diagrams 1091T and 1092T, it can be seen that they are very similar to one another for Octal or Hexidecimal entry. The Hexidecimal(1091T) uses as its timing control a 4 bit shifting action as can be seen by the Clock in the center of the Drawing label SHIFT with a single load bit. The function is initiated by receipt of Keystroke from the Data Entry Keyboard. A bounce delay smooths out the input Keystroke so that no transients are present; and on the trailing edge, an Input Strobe is initiated which sets a Clock Memory. The Clock Memory, becoming set, turns on the Clock, which starts a shifting action to move a Sequence Generator through five locations. The first activity required in the control system is to shift for four Clock cycles, the the data which was previously stored in the Data Register. Upon receipt of the fourth shift line, a Load Memory is set, which then is gated with the Clock line that allows the data which was being presented by the input Keystroke, to be loaded in parallel into the Data Register. Upon seeing the fifth sequence Control Bit (Bit E), the Clock Memory is cleared, and the entire System is terminated into a wait condition for the next Keystroke.

Octal Timing - Similar to Hexidecimal, the Octal Timing Diagram shows the data entry from a Keystroke which passes through a bounce delay and upon the trailing edge, an Input Strobe is initiated which sets the Clock Memory. The purpose of the bounce delay is on the trailing edge of this waveform, the Keystroke input data must remain in a positive condition, which is gated then to cause an Input Strobe to Occur. It can be seen on the second bounce delay that the Keystroke is false; therefore, no Input Strobe occurs. The Clock is started which contains one less clock pulse than previously defined for Hexidecimal, which allows three Shift pulses plus one load pulse. The Sequencer contains five bits; however, the A Bit and B Bit are loaded to a high condition in Octal with the receipt of Input Strobe. Therefore, the first clock pulse allows Bit C to become high, the second clock pulse allows Pin D to become high and the third clock pulse allows Pin E to become high.

2.11.2

DETAILED DESCRIPTION, KEYBOARD ENTRY, & DATA REGISTER DISPLAY

Referring to Drawing 1117 at the end of this addendum, Keyboard Input Data arrives at the upper center of the Drawing on Pin LL (Bit 1), Pin 32 (Bit 2), Pin 34 (Bit 4). and 35 (Bit 8). These lines are normally held Low through 100 ohm resistors to ground and as the input data arrives as a positive or +5 level via the diode modules previously defined, the true condition therefore turns off inverters U14 which are presented into the data in/out invert gates U7. The common or'ed Clock arrives on Pin 36 at the lower center of the page as a positive pulse. This positive level steers the Set Pulser U5 Pin 2 to high and also enables the Bounce Delay one shot U1 Pin 4 in motion. This one shot is approximately 2 miliseconds in duration, and on the trailing edge of the one shot, the Set Pulser U5 Pin 3 is tested, which when the Keyboard Strobe Input is High, will set the Strobe Pulser to ON.

The Set Pulser, becoming ON, causes U5 Pin 6 to become Low, driving the Clock Memory U5 Pin 9 to High. The Clock Memory setting, directly resets the Set Pulser so that the end result of the Set Pulser was a trailing edge Bounce Delay spike presented into the Clock Memory.

The Clock Memory becoming set, releases a clamp on the Sequencer Controller, U2, the reset input on Load Memory U6 Pin 1, enables the Clock tp begom free nning (U1 Pin 10), and releases the clamp on the Clock Binary U8 Pin 1.

The Clock, when running, is applied to the Clock Binary for a divide by two square wave generation, and continously tests the Invert Memory U8 Pin 11. The Clock Binary output is presented as Clock Input to the Data Output Register, for shifting as controlled by the SHIFT/LOAD input switch (Load Memory). The Clock will begin shifting the Data Output Register until the load Memory has been set. On the leading edge of each Clock Binary Cycle, the Output Data Register is shifted and on the trailing edge, the Clock Memory is tested to see if the cycle complete has occurred, and also allow the Sequence Control Generator U2 to shift once increment position. If JPI is inserted (for Hexidecimal) on the Sequence Control Pin U3 Pin 2, the preset load condition of the Clock Memory setting will cause the A input being High to set its High into the output line AO of the Sequence controller (not shown). This means in effect that the Hexidecimal mode of operation, fourClock pulses are required in order for E subzero to become High, setting at that time the Load Memory U6 Pin 6 to Low, This causes then the Memory to be selected into the Load condition so that the following Clock Pulse will receive the data from the Data Input Invert Gates, presented through the data play back or'ed gates U16 into the data input of U17 Pin 4,5,6, and 7. A true is a plus is a bit into the Data Shift Register U17.. A true condition will set the four bits of information into the output QA through QD at the Clock Time. As the Load Memory is set, the Clock Memory is now steered on U5 Pin 12 to Low so that the trailing edge of the Clock Binary, testing the Clock Memory, shall cause it to clear, thereby stopping all operation and returning the Sequence Control Shift Register back to its initialized state. Each Keystroke accomplishes the preceding timing arrangement so thatthe net effect is four shift pulses and one load pulse for each Keystroke entry

DISPLAY- The Output Data Register presents its eight bits through Data Invert Display Gates U11 and U9 to the LED Front Panel Display, shown in the upper right hand corner of the Drawing. The exclusive or'ed arrangement is utilized for inverting the data on a complement basis.

Word Clear-During the process of inputting a word into the Data Shift register, the C subzero Bit U2-13 of the Sequence Controller when High, causes a Word Clear to occur, thereby resetting the data which was resident in the Control Card Data Register. Since the Keyboard Strobe Line Pin 36 is High at this time, CR2 will conduct which drives the Clear Gate into an OFF state (U19 Pin 1), therefore the Word Clear command issued from Inverter U13 Pin 10 doesn't pass through the Clear Gate to clear the resident Output Data Register.

As the function has completed itself with the Clock Memory becoming reset once again, the emitter of Transistor Q1 is brought again to ground. The collector is referenced to the "Load F" buss, whose output is presented along with Keyboard Strobe turning ON Q1 as a test pulse to drive the Data Output Gates U18 and U25, into the K1 lines of the Control Card, directly setting the data into the Output Data Buffer of that Control Card.

In this way, each Keystroke updates the Control Card Data Register, therefor Word Clear from the keyboard is not required to enter a new word into the Control Card Data Buffer.

2.11.3

PLAYBACK AND DISPLAY

The Data Input Lines, located at the top of the Drawing on Pins M through V, are applied to Data Input Set Gates, U22 and U15. A Low on the Input Buss equals a bit, and when coupled with a Read Pulse from the buss structure, arriving on Pin X, (on the left hand side of the Drawing), this pulse shall couple through the Read Strobe Gate U19 Pin 6 so that the trailing edge of the gate will set a pulse R14 Pin 6 and Load Memory U6 Pin 8. The Load Memory becoming set, enables the Data Input Set Gates so that the information from the data input buss is therefore presented through data orgates into the Output Data Register directly. The Read Load Memory directly sets the Load Memory, and sets the Clock Memory via capacitor resistor network C6, R5, and R1. As the Clock Memory sets, and the Clock is started, since the Load Memory is in its set state, Only a Load Pulse occurs without shifting, and one Clock Pulse from the Clock Binary will then test the Clock Memory and reset it after the first Clock has occurred. Therefore, a jam type input from the Data Input Buss through the Data Input Set Gates and into the Data Output Register occurs on a playback basis.

2.11.4

TRANSLATOR CONVERSION

When the translator is selected for conversion, Pin 25 or Translator Enable, is brought to ground from the Control Card. This line becoming Low, falsifies the Read Strobe Gate U19 Pin 5 via Inverter U13 Pin 6, and sets the Busy Memory U12 Pin 6 to Low, thereby causing Translator Busy to occur on Pin BB. The Translator will remain Busy, causing the Control Card to operate in its "Translator Jump Loop" with Input data into the Translator arriving on Data Output Buss, Pins 11 through 18, and are presented to the two PROM's U21 and U20. Data is converted from ASCII to Hexidecimal with the PROM U21, and the Control Sequence is generated by PROM U20. No conversion will occur until the Start of Message, U20 Pin 10, occurs to set the SOM Memory U12 Pin 9 to ON. This Memory becoming set, therefore allows the Busy Clear Gate to be interrogated by the receipt of Space from the PROM U20. Data conversion allows information to be presented in parallel to the Keyboard Input Data previously described, which is presented to the Output Data Shift Register, U17 Bits A, B, C, and D. Each data word detected from U20 Pin 12 initiates a Clock Cycle, by driving the Set Pulser U5 Pin 4 to ON via capacitor C6, therefore a Clock Cycle occurs in identically the same manner as previously defined. Data will be shifted and then loaded until a Space Code is detected, which clears the Busy Memory, dropping BB off of Busy, and allowing it to become High. This function allows the Control Card to again release itself from a "busy conversion loop," and then process the information which is resident in the Control Card Data Buffer. As soon as that information has been stored, Translator Enable is again initiated to start conversion once again. This process will continue until EOM occurs which cancels the SOM Memory.

Word Clear on the Control Card Buffer is accomplished in identically the same manner as previously defined, due to the fact that the Busy Clear Gate, U19 Pin 8, becoming Low, passes into the cable "reference A," which is connected to the Word Clear Memory, U3 Pin 4. When this Memory sets, Word Clear is initiated, which drives the Control Card Buffer into a cleared state. Data is driven into the Control Card as soon as the Translator Enable line has been falsified or becomes High (Pin 25), into cable "reference C," which is connected through capacitor C13 to inverter U14 Pin 1 in the lower right hand corner of the Drawing.

The programs for both RPOM's U21 and U20 are located in the left lower corner of the Drawing for clarification.

2.11.5

DATA TRANSLATION EXAMPLES

The following examples of Hexidecimal Format show data being prepared in High and Low order Format. A Paper Tape sample is enclosed as Figure 1 at the end of this section showing a sequence of data words for preparation. The first word for any acceptable Hexidecimal Format must be a Start of Message word (Channel 1), which activates the Translator. After SOM occurs, the Translator investigates the inbound data, converts it to internal Hexidecimal Format and accepts the preceeding two words from the Execute command (Space) as the converted word.

The Input data words which are acceptable as data are converted to Hexidecimal as follows:

TABLE I

INPUT WORD	INPUT ASCII CODING	HEX CONVERSION
0	56	8421
1	56	0000
2	56	0001
3	56	0010
4	56	0011
5	56	0100
6	56	0101
7	56	0110
8	456	0111
9	456	1000
A	7	1001
B	7	1010
C	7	1011
D	7	1100
E	7	1101
F	7	1110
		1111

The tape example contains the ASCII data as indicated on the edge of the tape sample. Each word represents the High order followed by low order.

The 8 Bit word formed by two Hexideciaml words appears as below.

TABLE 3

	8 7 6 5 4 3 2 1
Ø1 =	1
1Ø =	5
35 =	6 5 3 1
AF =	8 6 4 3 2 1
78 =	7 6 5 4

OCTAL FORMAT

Octal is identical to Hex except that Octal requires 3 words to form an 8 bit word with all bits being 377.

	HI	MIDDLE	LOW	ORDER
	8 7	6 5 4	3 2 1	
Ø31		5 4	1	

The legal acceptable characters for Octal are Ø - 7 only. The High order word will not exceed 3, and if a 7, for example, is presented as the High order word, the 4 bit will be rolled off. A sample Octal tape format is attached as Figure 2.

FIGURE I

8 Bit Format (1)

BINARY EQUIVALENT

HI 8 7 6 5 4 3 2 1 LO

5 1

6 2

6 5 2 1

7 3

7 5 3 1

7 6 3 2

7 6 5 3 2 1

8 4

8 5 4 1

8 6 4 2

8 6 5 4 2 1

8 7 4 3

8 7 5 4 3 1

8 7 6 4 3 2

8 7 6 5 4 3 2 1

1

5 2

6 2 1

6 5 3

7 3 1

7 5 3 2

7 6 3 2 1

7 6 5 4

8 4 1

8 5 4 2

8 6 4 2 1

8 6 5 4 3

8 7 4 3 1

8 7 5 4 3 2

8 7 6 4 3 2 1

NOTES: (1) 4 Bit format uses only one stroke of data, rather than two.

(2) Only two strokes of data preceeding space are accepted. Additional bites preceeding space are not recognized.

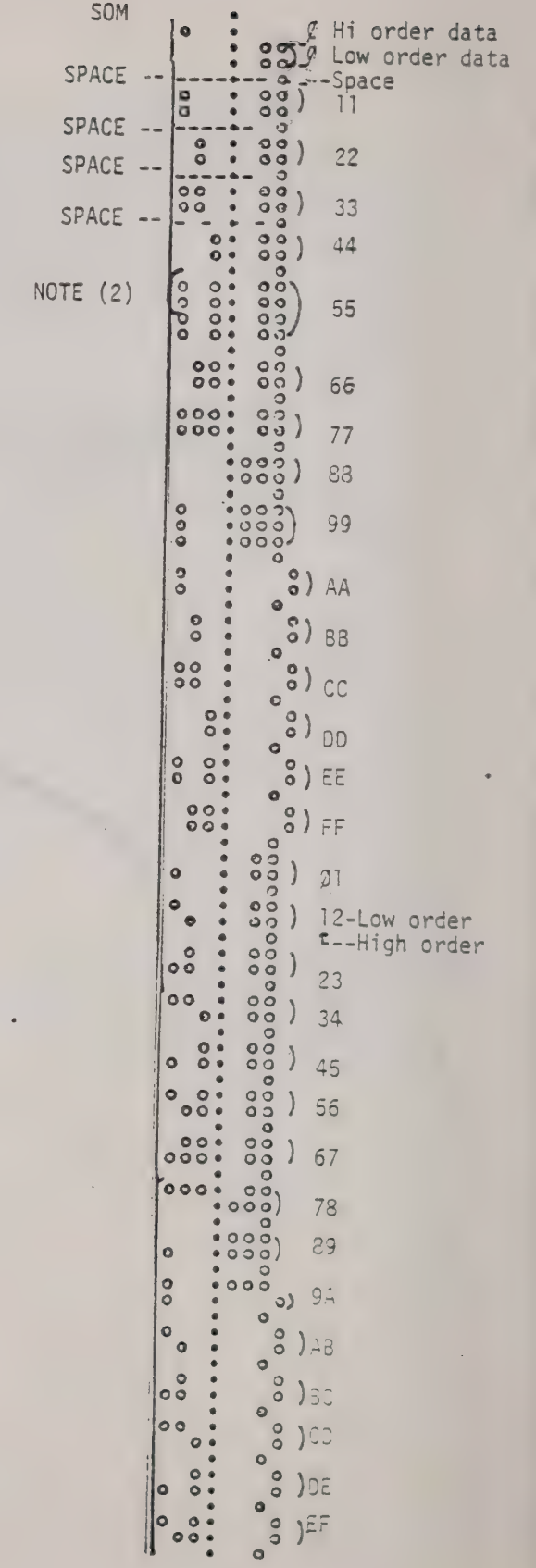
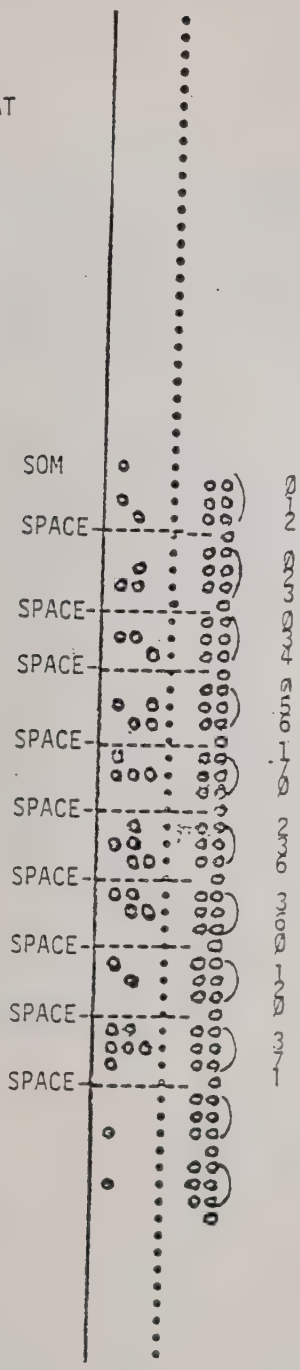


FIGURE 11.

(1) 8 Bit FORMAT



Binary Equivalent

High			Middle			Low	
8	7	6	5	4	3	2	1
				4		2	
			5			2	1
			5	4	3		
		6		4	3	2	
	7	6	5	4			
8			5	4	3	2	
8	7	6	5				
	7		5				
8	7	6	5	4			1

NOTES: (1) 4 bit format may be accomplished with one or two strokes of data, rather than three.

(2) A maximum of three strokes of data before Space is recognized. Additional bites preceeding Space will not be recognized.

SECTION 3
POWER SUPPLY

3.0 Power Supply

3.1 General Description

The Power Supply converts the A.C. line voltage of 115/230 volts + 10%, 50-60 Hertz, single phase, into the six D.C. voltages required by the Data I/O Programmer. These voltages, +5, -9, -5, +24, + Programmable, and the floating 48 volt supply are all controlled by 723 Precision Voltage Regulators. Each circuit is set up with current limiting and short circuit protection. The Power Supplies limit at the following currents:

+5	.5 Amperes
-9	.500 Milliamperes
-5	.250 Milliamperes
+24	1.2 Amperes
+ Programmable	1.2 Amperes
Floating 48 Volts	1.0 Amperes

3.2 Power Supply Operation

(Refer to schematic 1087)

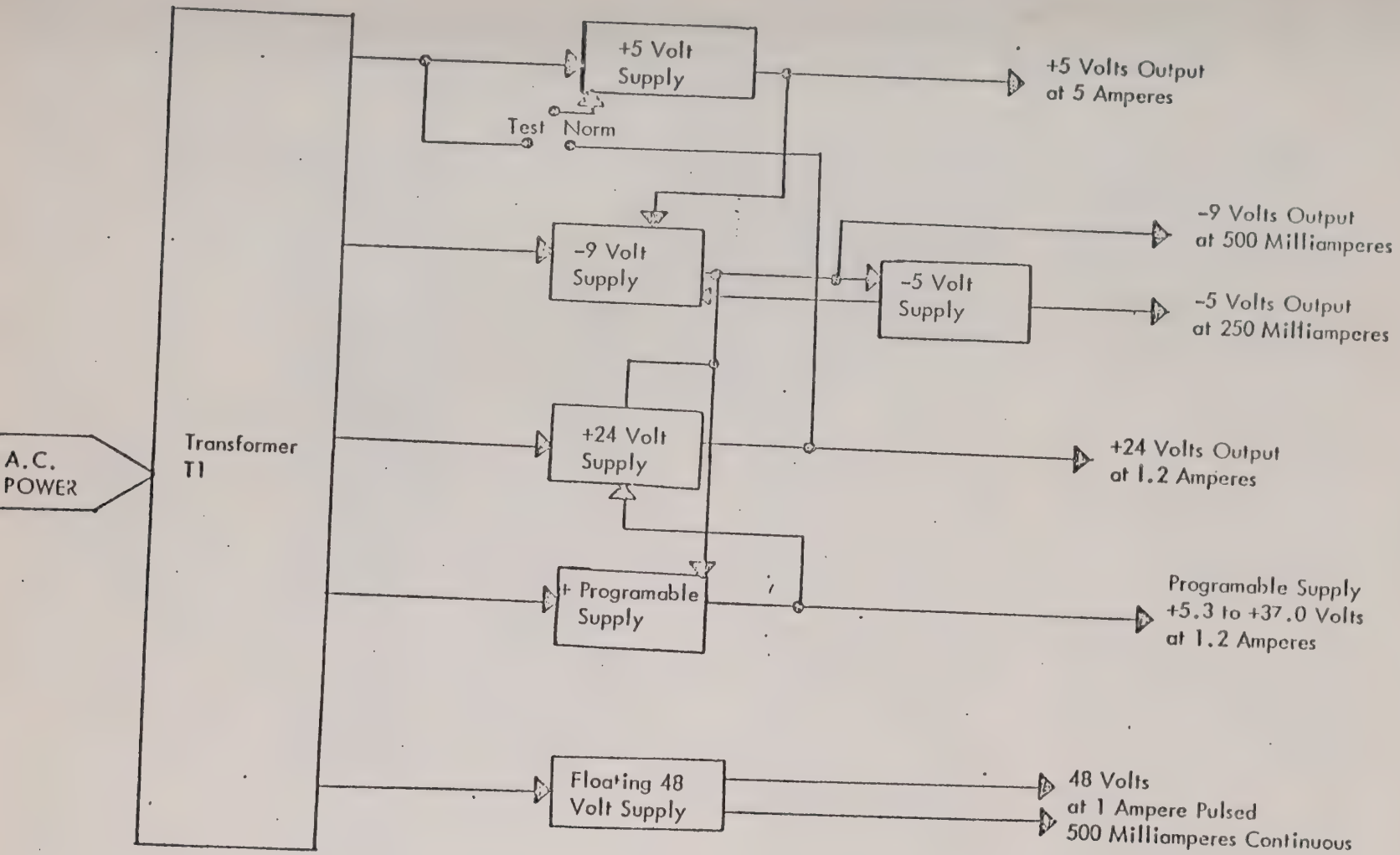
3.2.1 Short Circuit Protection

The +5, -9, -5, +24 and +Programmable Supplies are interconnected as shown in the block diagram on the following page. As a result of this type of loop, one voltage is dependent on another voltage to ensure that the voltage remains at its proper voltage level. Therefore, a short on any voltage output to ground will shut down the next voltage in the loop until all of the voltages are shut down. This provides protection for the power supply against supplying maximum current for any length of time. After the short has been removed the Power Switch has to be switched off; after the capacitors have discharged, switch back to on to start the power up sequence. A test jumper has been provided to open the interconnecting loop for troubleshooting.

3.2.2 +5 Volts

A.C. current flows through the Primary windings of the transformer T1 when the Power Switch is in the On Position. The voltages are then developed on the secondary windings of the transformer; 9 volts RMS at 5 amperes across the blue leads, 10.5 volts RMS at 1 Ampere across the violet leads, 33 volts RMS at 1.5 Amperes across the yellow leads, and 50 volts RMS at 750 Milliamperes across the white leads. These voltages are applied through J1 to the A.C. inputs of the full wave bridge rectifiers D1, D2, D3 and D4. The D.C. output of D1 charges C13 to 12 volts, the D.C. output of D2 charges C14 to 14 volts, the D.C. output of D3 charges C15 to 70 volts, and the D.C. output of D4 charges C16 to 45 volts. As the voltage increases across C16, capacitor C18

BLOCK DIAGRAM


A.C. POWER
Transformer T1
+5 Volt Supply
Test
Norm
+5 Volts Output at 5 Amperes
-9 Volt Supply
-9 Volts Output at 500 Milliamperes
-5 Volt Supply
-5 Volts Output at 250 Milliamperes
+24 Volt Supply
+24 Volts Output at 1.2 Amperes
+ Programable Supply
Programable Supply +5.3 to +37.0 Volts at 1.2 Amperes
Floating 48 Volt Supply
48 Volts at 1 Ampere Pulsed 500 Milliamperes Continuous

is charged to provide a voltage ot the +V and Vcc inputs of the 723 of the +5 volt supply (U1) through the Jumper (JP1) in the "NORM" position. When the voltage at +V of U1 exceeds 9 volts, the 723 will operate providing a reference voltage of 7 volts at U1 Pin 6 and 2.5 volts at Pin 5 of U1 through the voltage divider R17 and R19. This causes the output voltage of the 723 to increase supplying base current to Q10 and Q10 supplies base current to series pass transistor Q1. As the voltage on Q1 emitter increases, the voltage on Pin 4 of U1 increases to 2.5 volts switching off the 723. The voltage divider of R15, R16 and potentiometer R18 is set up to supply a voltage of 2.5 volts on Pin 4 of U1 when Q1 emitter is 5.2 volts.

3.2.3 -9 Volts and -5 Volts

The +5 volts then supplies the voltage for the +V input of the -9 regulator (U2) causing the device to start regulating and Q2 to draw base current. Q2 turning on provides a ground reference for the -9 volt supply. The voltage on Pin 7 of U2 will become more negative as Q2 is turned on harder. Zener diode CR1 will clamp the voltage on the base of Q3 and Pin 4 of U2 at -5.6 volts. The base emitter junction of Q3 will drop .6 volts charging C1 to -5 volts. The inverting input at U2 Pin 4 being at -5.6 volts is used as a reference for the -9 regulator. The voltage divider of R7, R6 and potentiometer R40 is set up to have a voltage of -5.6 volts on Pin 5 of U2 when the minus side of the supply is at -9 volts.

3.2.4 + Programmable

With C16 charged to 45 volts and the -9 volt supply not at -9, current will flow through R44 and R43 to the base of Q4 and Q5, turning these two transistors on will hold pins 13 of U4 and U5 at ground, preventing the internal output transistors of U4 and U5 from turning on, therefore holding off the +24 volts and the + programmable supplies. When the -9 volt supply reaches -9 volts, the divider of R43 and R10 will cause the base of Q5 to go to -0.6 volts causing Q5 to switch off. This releases the internal output transistor of U5 and allows the voltage of the programmable supply to increase. The voltage divider of potentiometer R30, R9 and R8 is set up to provide a voltage of 5.3 volts on Pin 5 of U5 therefore, the programmable supply will increase to 5.3 volts with the sense and operate lines left open. When a program card is plugged into the Data I/O Programmer requiring a specific voltage, a resistor (Rxx) on the program card is either connected from the operate line to ground or from the sense line to the operate line and the operate line is tied to ground. This will set up a voltage divider with R3, R2, R1 and Rxx, requiring the voltage at Q8 emitter to increase to a specific voltage between 5.3 volts and 37 volts depending on Rxx value and how it is connected (See Fig. 1) to maintain 5.3 volts on Pin 4 of U5.

3.2.5 +24 Volts

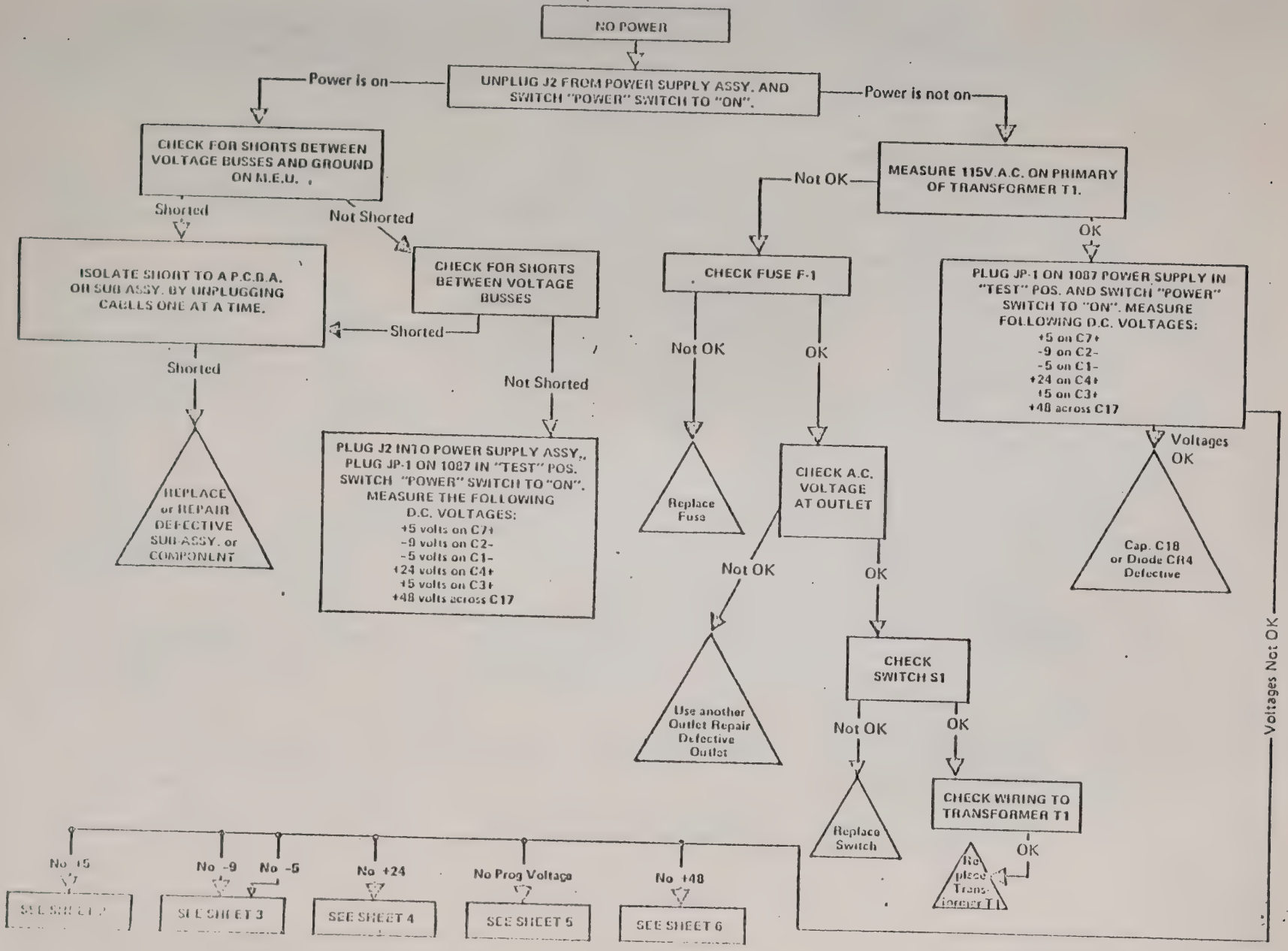
A the programmable supply voltage becomes more positive, current will flow thorugh R33 and Q13 base, turning Q13 on and switching Q12 off. With Q12 off and Q4 off, U4 pin 13 is allowed to go positive turning the internal output transistor of Q4 on. This allows the 723 to drive Q7 causing the emitter to go

positive, as Q7 emitter voltage increases, the voltage at U4 Pin 4 increases through voltage divider R27, R25 and R26 until the voltage at Pin 4 of U4 is the same as U4 Pin 5. The voltage divider is set up so Q7 emitter will be 24 volts at this time. The 24 volts on Q7 emitter will supply the voltage through CR4 to the +V input of U1 preventing the supply from shutting down after C18 has discharged.

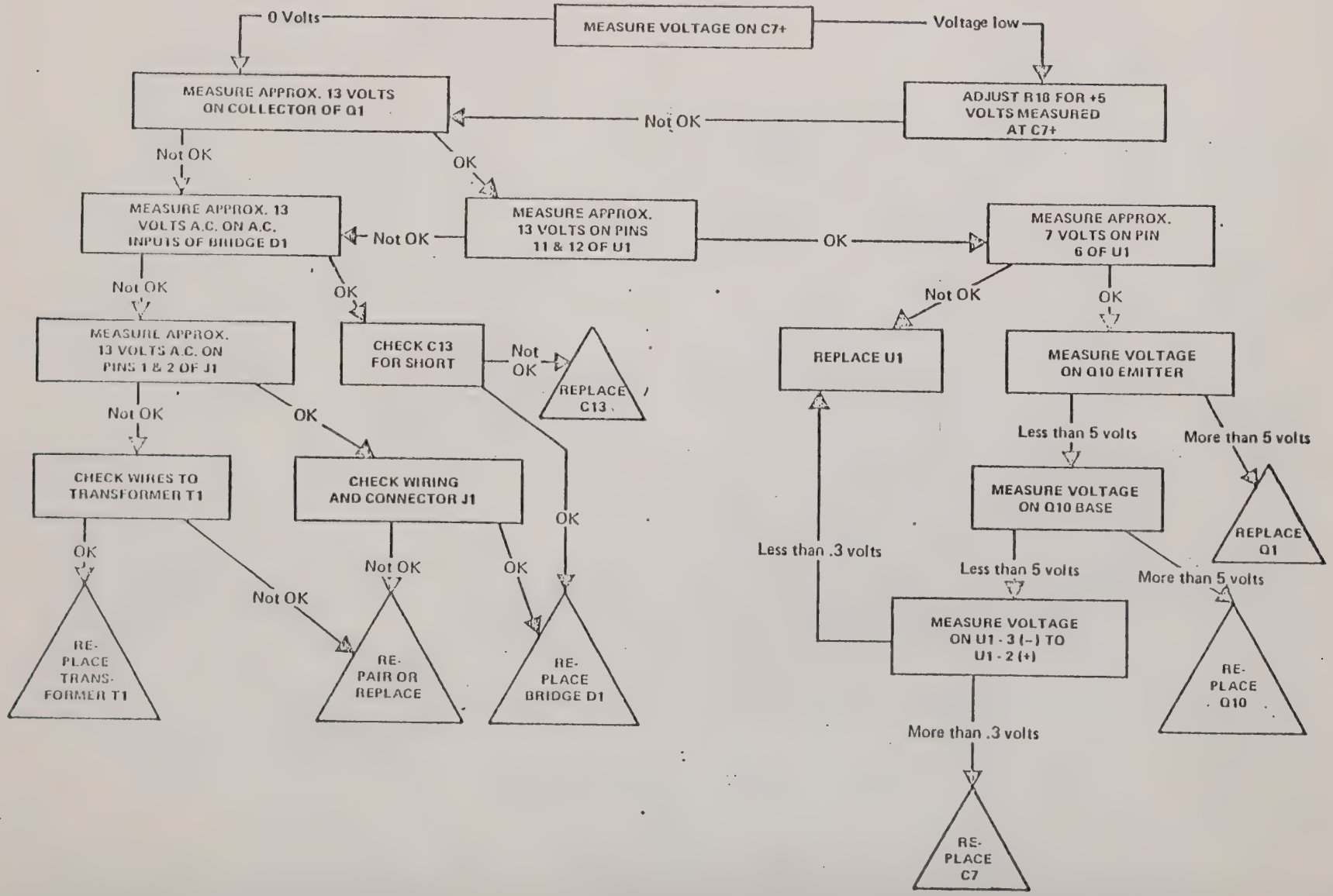
3.2.6 48 Volts

The floating 48 volt supply is isolated from the reset of the power supply and is not referenced to ground until J2 Pin 9 is connected to ground providing -48 volts at J2 Pin 5 or connecting J2 Pin 5 to ground providing +48 volts at J2 Pin 9. The floating 48 volt supply comes up independent of the other voltages. The D.C. output charged C15 to 70 volts, current flows through R20 and Zener diode CR2 clamping the voltage at +V and Vcc inputs of U3 to 24 volts. The output of U3 drives the base of Q9 which allows Q9 to sink base current from Q6, turning Q6 on until the collector reaches 48 volts. At 48 volts the voltage divider R12 and R23 provide a voltage on Pin 4 of U3 that will equal the voltage on Pin 5 of U3 resulting from the voltage divider R21, R22 and the adjustment of potentiometer R24. A current is drawn from the 48 volt supply, voltage is dropped across R31, if the current increases to 1.2 amperes the voltage across R31 turns on Q11 allowing current to flow through R32 and through the current limit circuitry of U3 causing the output voltage to decrease. This will continue until the current is decreased or F2 opens up protecting the components of the floating 48 volt supply from breaking down or damage due to excess heat.

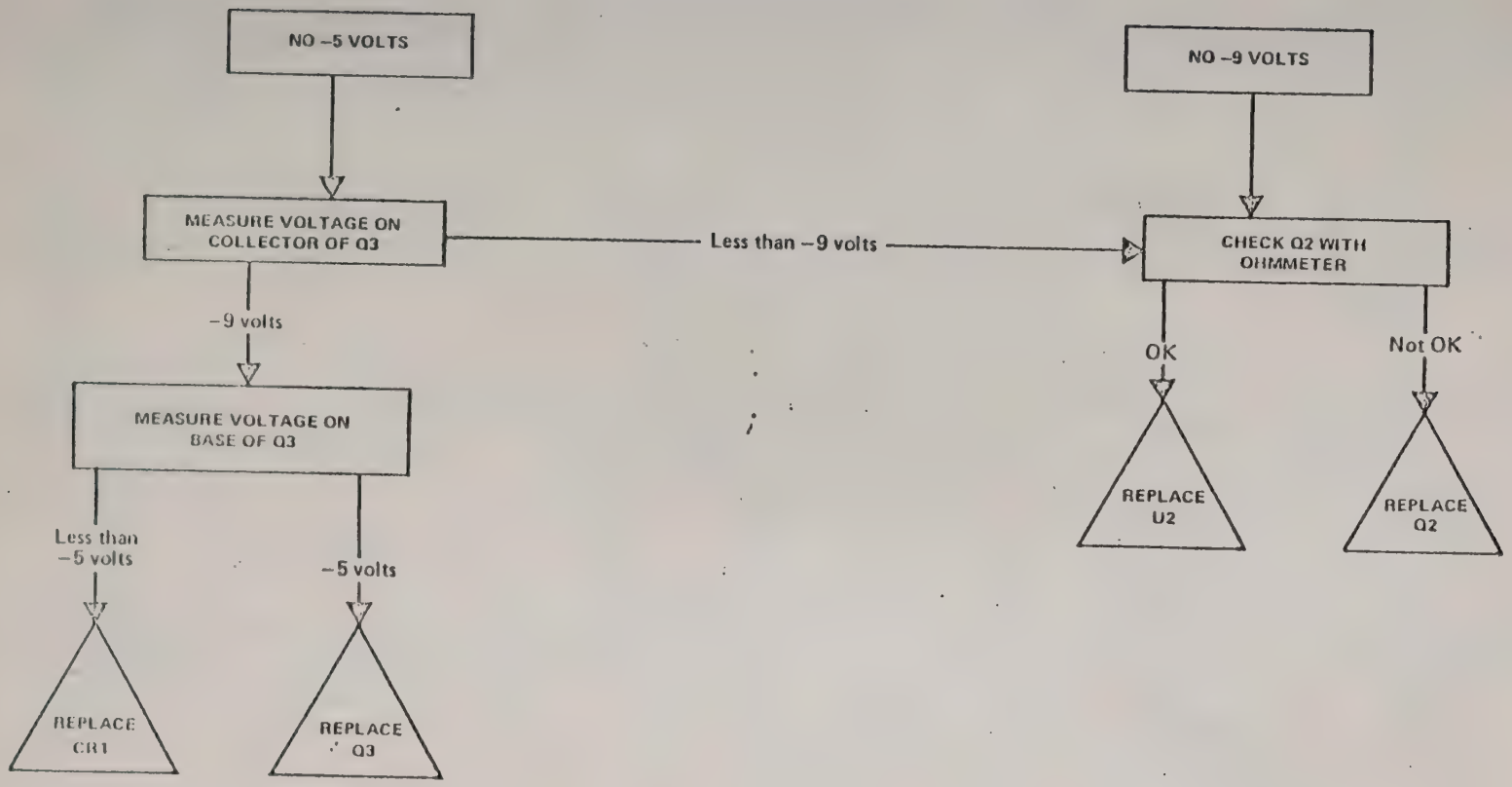
1087 POWER SUPPLY TROUBLESHOOTING DIAGRAMS


NO POWER
UNPLUG J2 FROM POWER SUPPLY ASSY. AND SWITCH "POWER" SWITCH TO "ON".
Power is on
Power is not on
CHECK FOR SHORTS BETWEEN VOLTAGE BUSSES AND GROUND ON M.E.U.
Shorted
Not Shorted
ISOLATE SHORT TO A P.C.B.A. OR SUB ASSY. BY UNPLUGGING CABLES ONE AT A TIME.
Shorted
REPLACE or REPAIR DEFECTIVE SUB-ASSY. or COMPONENT
CHECK FOR SHORTS BETWEEN VOLTAGE BUSSES
Shorted
Not Shorted
PLUG J2 INTO POWER SUPPLY ASSY., PLUG JP-1 ON 1087 IN "TEST" POS. SWITCH "POWER" SWITCH TO "ON". MEASURE THE FOLLOWING D.C. VOLTAGES:
+5 volts on C7+
-9 volts on C2-
-5 volts on C1-
+24 volts on C4+
+5 volts on C3+
+48 volts across C17
MEASURE 115V.A.C. ON PRIMARY OF TRANSFORMER T1.
Not OK
OK
CHECK FUSE F-1
Not OK
OK
Replace Fuse
CHECK A.C. VOLTAGE AT OUTLET
Not OK
OK
Use another Outlet Repair Defective Outlet
CHECK SWITCH S1
Not OK
OK
Replace Switch
CHECK WIRING TO TRANSFORMER T1
OK
Replace Transformer T1
PLUG JP-1 ON 1087 POWER SUPPLY IN "TEST" POS. AND SWITCH "POWER" SWITCH TO "ON". MEASURE FOLLOWING D.C. VOLTAGES:
+5 on C7+
-9 on C2-
-5 on C1-
+24 on C4+
+5 on C3+
+48 across C17
Voltages OK
Cap. C18 or Diode CR4 Defective
Voltages Not OK
No +5
No -9
No -5
No +24
No Prog Voltage
No +48
SEE SHEET 2
SEE SHEET 3
SEE SHEET 4
SEE SHEET 5
SEE SHEET 6

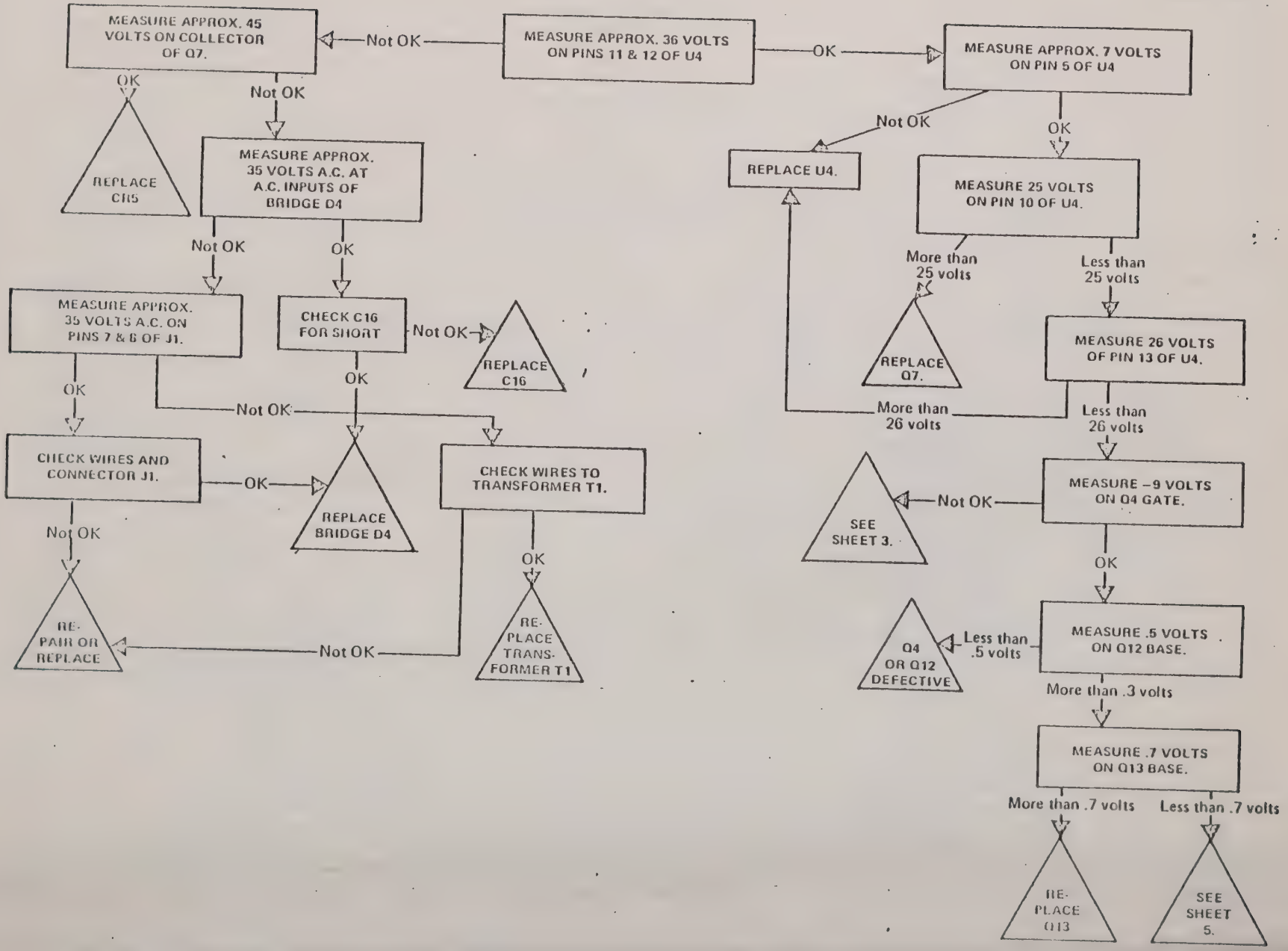
NO +5 VOLTS OR VOLTAGE TOO LOW



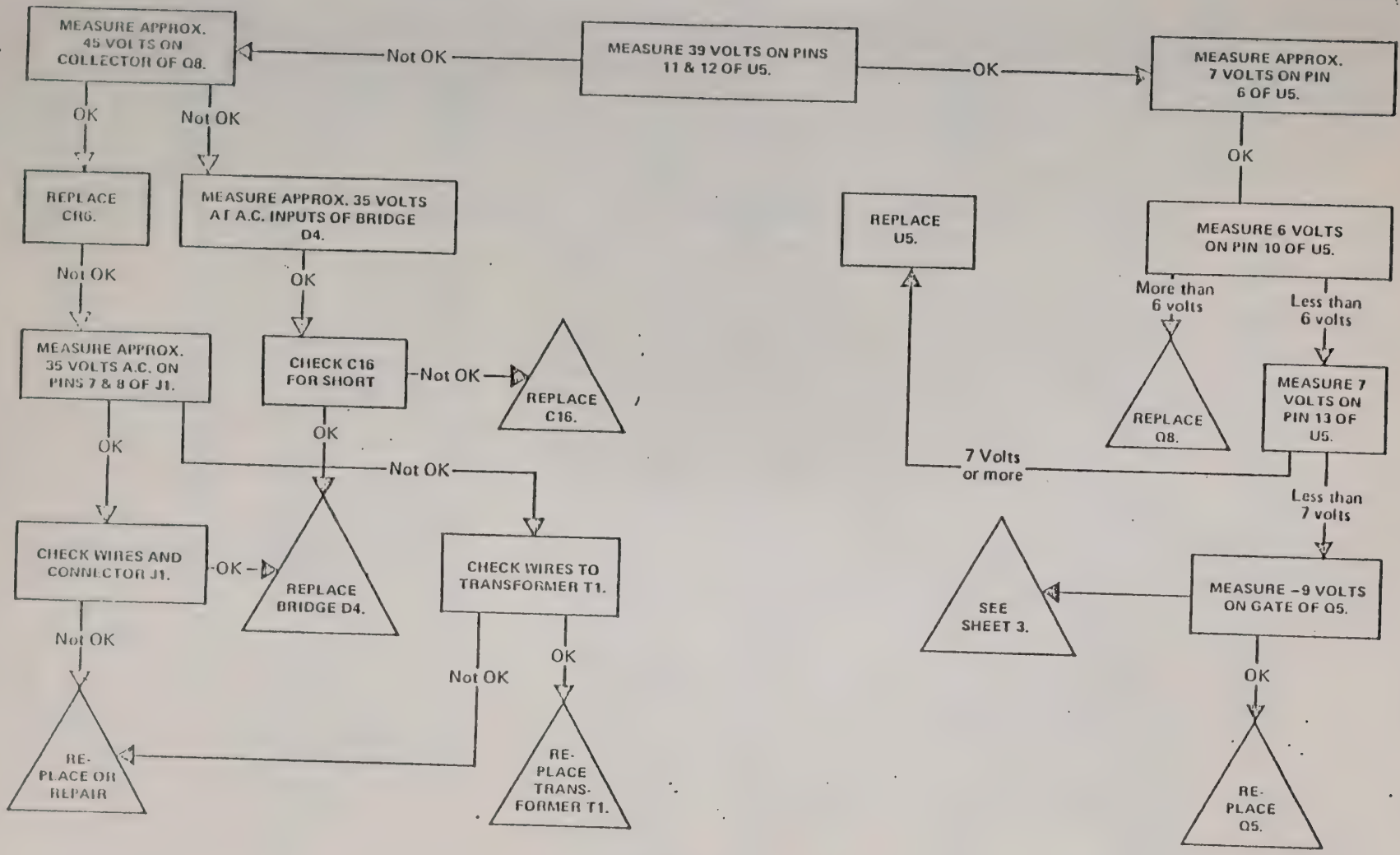
NO -9 VOLTS OR -5 VOLTS

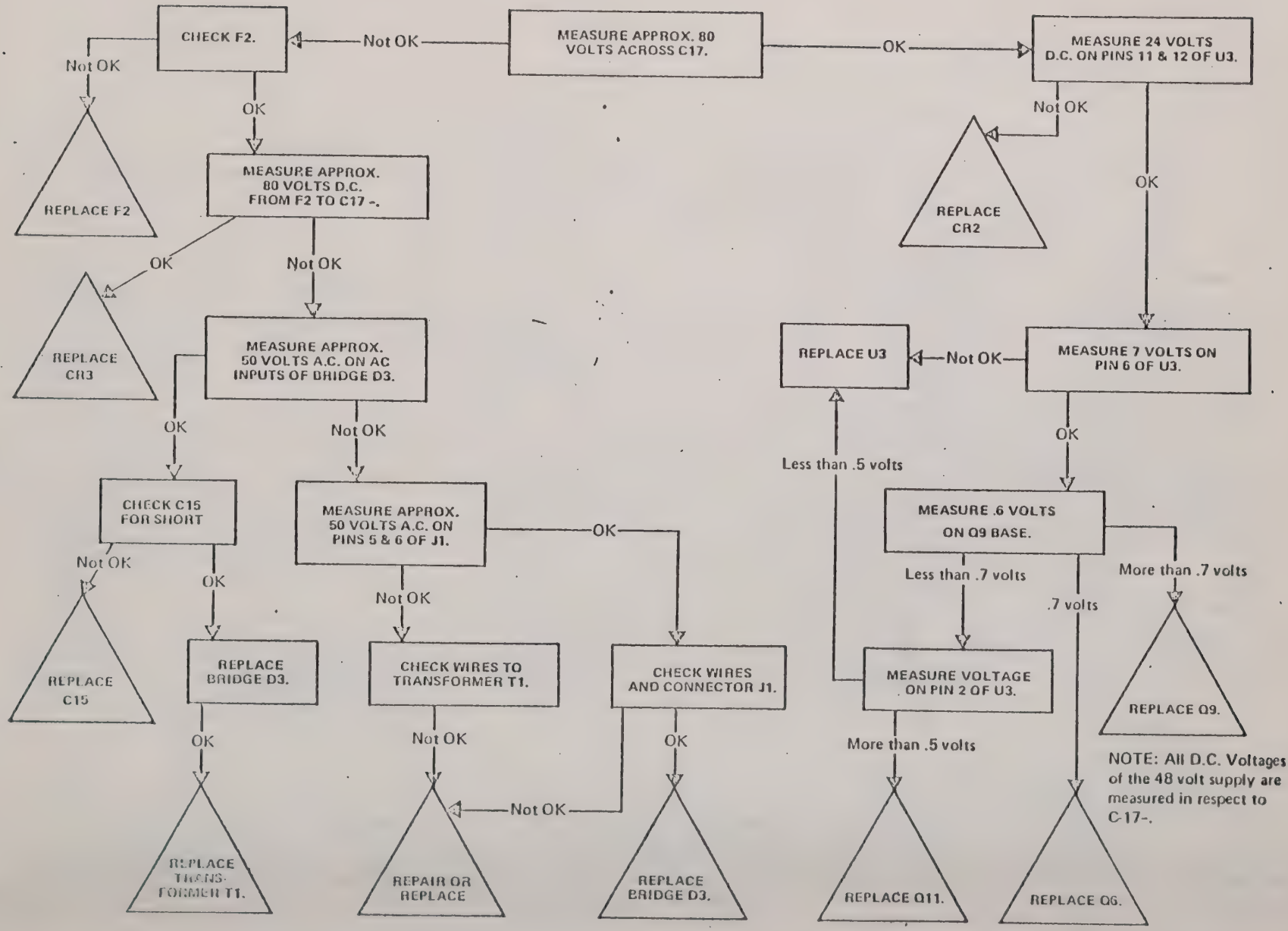


NO VOLTS


MEASURE APPROX. 45 VOLTS ON COLLECTOR OF Q7.
Not OK
MEASURE APPROX. 36 VOLTS ON PINS 11 & 12 OF U4
OK
MEASURE APPROX. 7 VOLTS ON PIN 5 OF U4
OK
REPLACE CR5
Not OK
MEASURE APPROX. 35 VOLTS A.C. AT A.C. INPUTS OF BRIDGE D4
Not OK
OK
MEASURE APPROX. 35 VOLTS A.C. ON PINS 7 & 8 OF J1.
CHECK C16 FOR SHORT
Not OK
REPLACE C16
OK
Not OK
CHECK WIRES AND CONNECTOR J1.
OK
REPLACE BRIDGE D4
CHECK WIRES TO TRANSFORMER T1.
Not OK
RE-PAIR OR REPLACE
Not OK
OK
RE-PLACE TRANS-FORMER T1
Not OK
REPLACE U4.
OK
MEASURE 25 VOLTS ON PIN 10 OF U4.
More than 25 volts
REPLACE Q7.
Less than 25 volts
MEASURE 26 VOLTS OF PIN 13 OF U4.
More than 26 volts
Less than 26 volts
SEE SHEET 3.
Not OK
MEASURE –9 VOLTS ON Q4 GATE.
OK
Q4 OR Q12 DEFECTIVE
Less than .5 volts
MEASURE .5 VOLTS ON Q12 BASE.
More than .3 volts
MEASURE .7 VOLTS ON Q13 BASE.
More than .7 volts
Less than .7 volts
RE-PLACE Q13
SEE SHEET 5.

NO + PROG \M VOLTAGE




MEASURE APPROX. 80 VOLTS ACROSS C17.
Not OK
CHECK F2.
Not OK
REPLACE F2
OK
MEASURE APPROX. 80 VOLTS D.C. FROM F2 TO C17 -.
OK
REPLACE CR3
Not OK
MEASURE APPROX. 50 VOLTS A.C. ON AC INPUTS OF BRIDGE D3.
OK
CHECK C15 FOR SHORT
Not OK
REPLACE C15
OK
REPLACE BRIDGE D3.
OK
REPLACE TRANS-FORMER T1.
Not OK
MEASURE APPROX. 50 VOLTS A.C. ON PINS 5 & 6 OF J1.
OK
CHECK WIRES AND CONNECTOR J1.
OK
REPLACE BRIDGE D3.
Not OK
CHECK WIRES TO TRANSFORMER T1.
Not OK
REPAIR OR REPLACE
OK
MEASURE 24 VOLTS D.C. ON PINS 11 & 12 OF U3.
Not OK
REPLACE CR2
OK
MEASURE 7 VOLTS ON PIN 6 OF U3.
Not OK
REPLACE U3
OK
MEASURE .6 VOLTS ON Q9 BASE.
Less than .7 volts
MEASURE VOLTAGE ON PIN 2 OF U3.
Less than .5 volts
More than .5 volts
REPLACE Q11.
More than .7 volts
REPLACE Q9.
.7 volts
REPLACE Q6.
NOTE: All D.C. Voltages of the 48 volt supply are measured in respect to C-17-.

Manual Addendum
for
Paper Tape Reader

4.0 The Paper Tape Reader mechanism is composed of a stepping motor with Sprocket, Photo Transistor Read Head and load resistors. The control of Reader motion and data detection is contained on the Data I/O Reader Driver Card, located in the Programmer card cage.

4.1 TAPE WIDTH

Multiple width tapes may be selected for use with the Reader by the small knob located on the front of the Reader. Programmers normally use 8 level tape only.

4.2 PERIODIC MAINTENANCE

The motor is lubricated for life, so no periodic maintenance will be required on the motor.

Using a soft cloth, brush, or a dry, clean air source, remove any accumulated dust and lint from around the tape guides, phototransistor cover and the LED assembly. This should be performed on daily basis to assure no read errors.

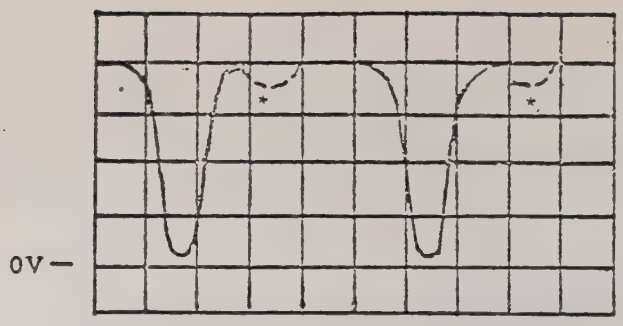
Every 4 months or 500 hours, inspect the reader for any obvious physical damage and tighten all screws that may have worked loose, including the two sprocket setscrews. Do not overtighten the screws holding the clear plastic covers on the LED's and phototransistors. The sprocket setscrews can be tightened by using a .035 in. Allen wrench through an access hole at the bottom of the reader.

4.3 ADJUSTMENTS

The sprocket is adjusted at the factory for proper operation bi-directionally with a light to medium symmetrical tape load. A heavy or non-symmetrical tape load may necessitate a sprocket adjustment.

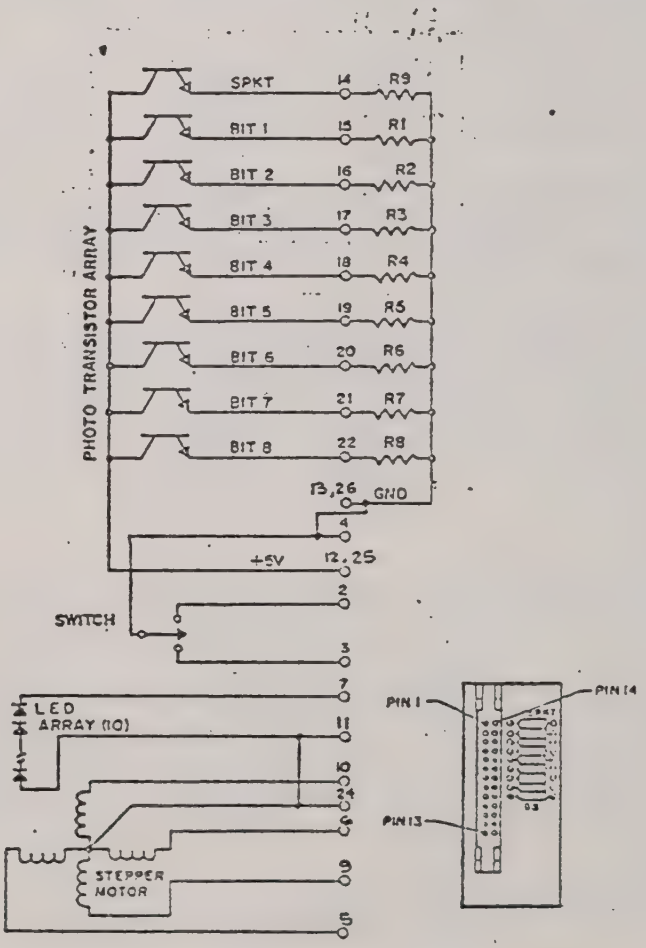
The sprocket adjustment can be accomplished by running tape under normal use conditions and monitoring with an oscilloscope the voltage across R9, the sprocket phototransistor emitter resistor. Slightly loosen the 3 motor hold-down screws and rotate the motor until the waveform is identical for both directions of tape motion and approximates that as shown in the illustration below. Retighten the moter screws.

CAUTION: The normal operating temperature of the motor can approach 100 C(212 F).



Normal sprocket signal at phototransistor
SCOPE VERT: 0.5 V/DIV SCOPE HORIZ: 2MS/DIV
SCOPE TRIG: CLOCK trailing edge
CLOCK RATE: 120 pps

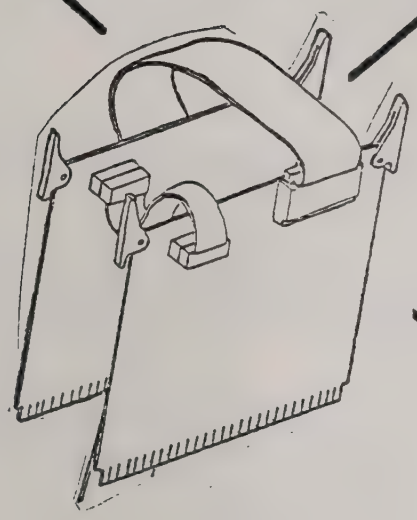
*May occur with a light tape load



SCHEMATIC-CONNECTOR BD.

ADDMASTER 601-2 READER (20057-2)

DATA I/O



OPERATOR MANUAL

Program (Personality) Card Set

PROGRAM (PERSONALITY) CARD SET
Description - Initialization - Operation

INTRODUCTION

This manual will assist the operator to install the Personality Card Set, the pROM Socket Adapter, and to make polarity and address limit determinations.

GENERAL DESCRIPTION

DATA I/O manufactures a wide variety of program cards capable of programming the many configurations and technologies of pROMs presently available.

The enclosed Comparison Chart shows these various pROMs, their configurations, and manufacturer's part number; DATA I/O Personality Card part number; Read Only Card part number; and pROM Socket/Socket Adapter to be used with them.

Program (Personality) Card Sets consist of two circuit board assemblies connected together with a 16-pin cable as shown in Figure 1D and 1E. The Digital Card (Figure 1E) contains all programmer logic interface and pROM program timing circuitry. The Analog Card (Figure 1D) contains all voltage switching and current limiting circuitry required for programming pROMs. The Digital Card controls the Analog Card through the connecting interface cable 709-1608 while the Analog Card provides pROM programming signals to the pROM Socket receptacle and Adapter (Figure 1A and 1B) through shielded cable 709-1012.

In general, the program cards are of two types; namely, Standard Program Cards, or Generic Program Cards (Comparison Chart note 5). These program cards are compatible for use in all series I, II, III, and $\overline{V}$ DATA I/O Programmers. The Standard Program Cards are capable of programming one type of pROM only and always use a standard socket adapter. Generic family program cards are capable of programming the specific manufacturer's generic family. Each different configuration of generic pROM may be programmed by installing the appropriate socket adapter (Figure 1B) indicated on the Comparison Chart.

When the enclosed operating instructions are followed, the program cards will deliver the programming yields specified by pROM manufacturers -- typically, in excess of 80%. Whenever a decrease in programming yield is experienced, the program cards should be recalibrated according to the applicable DATA I/O Calibration Chart. These calibrations are easily implemented with a DATA I/O Calibrator. The programming specifications are given in the DATA I/O pROM program specifications sheets which accompany the calibrator.

Another means to further improve programming yield is to use the Production Sequencer Option (950-0028). This option provides single button operation, continuity testing before programming and programming process indication.

INSTALLATION

With main Programmer power off, install the Digital Card (Figure 1E) in the ROM 2 position as shown in Figure 1. Simultaneously install the Analog Card (Figure 1D) in the spare Analog position. Note that the color coding of card guides and extractor tabs must agree for all card positions. Be certain that interconnect cable 709-1608 is firmly attached and Pin 1 is connected to Pin 1 on both ends.

Next, install the 709-1012 shielded cable between the Analog Card and socket receptacle (Figure 1A). Again, be certain that Pin 1 is connected to Pin 1 at each end. This is verified by the red or white marks identifying the Pin 1 side of the cable and cable connector socket.

The appropriate standard socket or socket adapter (Figure 1B) is then installed. For the correct socket refer to the attached comparison chart.

OPERATION

The Personality Card Set is capable of both programming information into and reading information out of a pROM when Program is selected. For more detailed program operation, refer to the Operator Section of the Programmer Manual.

C A U T I O N

Remove pROMs from Programmer socket before turning Programmer power ON or OFF.

ADDRESS LIMIT

Maximum address count in the Programmer is determined by the address limit select jumper on the Digital Card (Figure 1E) or by the Socket Adapter (Figure 1B). The Programmer will always respond to the lowest address limit present.

On all Standard Program Cards, the Address Limit is determined by the Address Limit Select Jumper (Figure 1E). Always be sure the Address Limit is set to agree with pROM configurations. For example, on a 256x4 pROM, select 256 Address Limit; and for a 512x4 pROM, select 512 Address Limit.

If a Generic Program Card is being used, the Address Limit on the Digital Card (Figure 1A) should be set to the maximum address available in the specific family. Shorter address limits for shorter address length pROMs within the generic family, are automatically selected by the pROM Socket Adapter. This socket adapter also automatically selects the pROM word width. For example, when a generic pROM of 256x4 configuration is selected by the pROM socket adapter, 256 Address Limit is selected along with Programmer data word width, which in this case will be a 4-bit BYTE.

B. **DIGITAL CARD** (701-1348)

1. Replace the timing PROM (U2) with a 32x8 open-collector PROM programmed per the truth table in Figure 4.

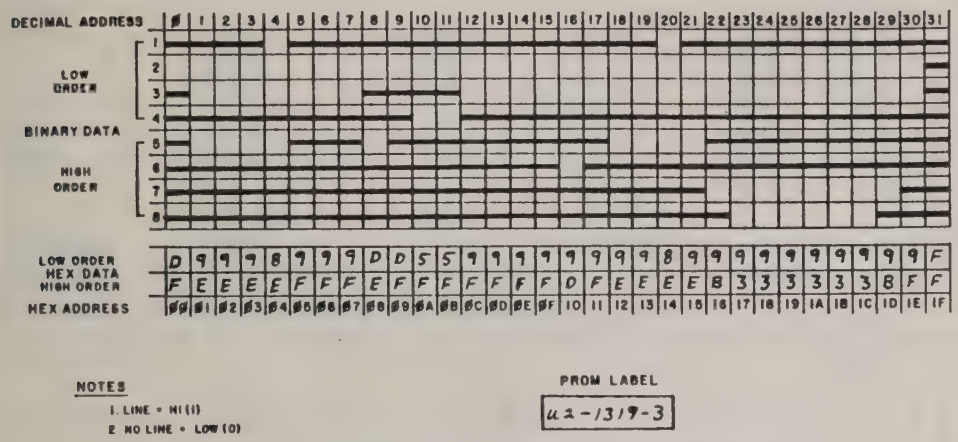


Figure 4. Truth Table for the Timing PROM

C. **CALIBRATION ADAPTER** (910-1319-3)

1. Replace the U1 (C1) PROM on the calibration adapter with a 32x8 tri-state PROM programmed per the truth table in Figure 5.

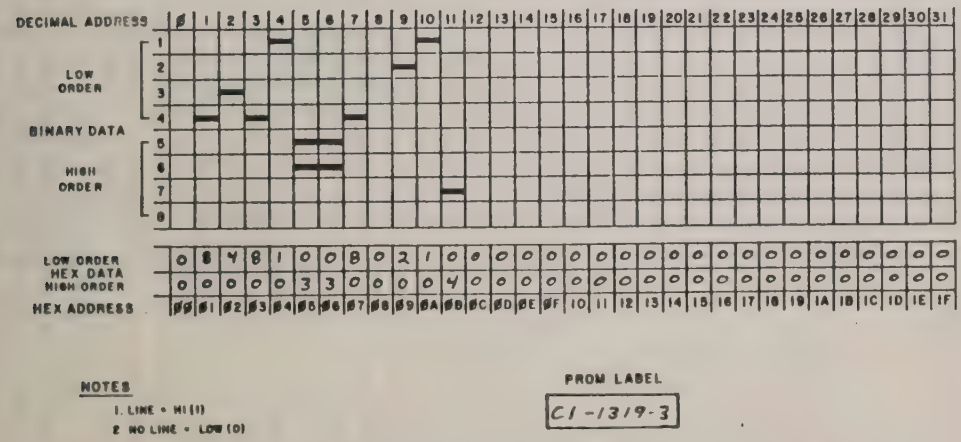


Figure 5. Truth Table for the Calibration-Adapter PROM

D. **CALIBRATION**

1. Recalibrate the card set per the enclosed calibration chart and timing diagram. Refer to your card set manual for the calibration procedure.

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1319-3 | PROGRAM CARD 909-1319-3
FIXTURE 702-1071 | MANUFACTURER HARRIS SEMICONDUCTOR
PAGE 1 OF 2 | PROGRAM ADAPTER 910-1319-3 | PROM HM 6611/61

DATE	REV	REVISION RECORD	DR	CK
4-79	B	ECN #2565	FS	
5-14-80	C	ECN #3345	KJB	KB

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U1	U2	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
00	44	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5
00	44	Power +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8
00	44	Supply +5	1-3	000	00	000			+5	R18	5.05	5.1	5.15
00	44	-9	1-4	000	00	000			-9	R40	-8.8	-9.0	-9.2
00	44	Prog V	1-5	000	00	000			+Prog		21.0	21.6	22.0
00	44	VCC Program (1)	2-1	000	00	000	5	1	3	R11	10.0	10.5	11.0
00	44	VCC Current Limit	2-2	000	00	000	6	1	3		0.0		0.4
08	44	VCC Verify	2-3	001	01	001	5	1	3	R9	3.0	3.5	4.0
04	44	VCC Read	2-4	002	02	002	5	1	3	R66	4.75	5.0	5.25
08	44	Comparator Reference	3-1	003	03	003			U5-P8		1.4		2.1
01	44	$\overline{CE}$ Level	4-1	004	04	004	7	5	3		0.0		0.4
30	44	$\overline{PE}$ Program (3)	4-2	005	05	005	7	6	3	R4	-19.5	-20.5	-21.5
30	44	$\overline{PE}$ Current Limit	4-3	006	06	006	6	6			0.0		0.4
08	44	PE Verify	4-4	007	07	007	4	6	3		3.0		4.0
00	44	CP High (2)	4-5	008	08	010	7	7	3		9.0		11.0
02	44	CP Low	4-6	009	09	011	7	7	3		0.0		0.4
01	C4	Bit 8 Program	5-1	010	0A	012	7	8	3		0.0		0.4
01	C4	Bit 7 No Program	5-2	010	0A	012	7	9	3		10.0	10.5	11.0
01	C4	Bit 6 Program	5-3	010	0A	012	7	10	3		0.0		0.4
01	C4	Bit 5 No Program	5-4	010	0A	012	7	11	3		10.0	10.5	11.0
01	C4	Bit 4 Program	5-5	010	0A	012	7	12	3		0.0		0.4
01	C4	Bit 3 No Program	5-6	010	0A	012	7	23	3		10.0	10.5	11.0
01	C4	Bit 2 Program	5-7	010	0A	012	7	22	3		0.0		0.4
01	C4	Bit 1 No Program	5-8	010	0A	012	7	21	3		10.0	10.5	11.0
01	C4	Bit 8 No Program	5-9	010	0A	012	7	8	3		10.0	10.5	11.0
01	C4	Bit 7 Program	5-10	010	0A	012	7	9	3		0.0		0.4
01	C4	Bit 6 No Program	5-11	010	0A	012	7	10	3		10.0	10.5	11.0
01	C4	Bit 5 Program	5-12	010	0A	012	7	11	3		0.0		0.4
01	C4	Bit 4 No Program	5-13	010	0A	012	7	12	3		10.0	10.5	11.0

COMMENTS

Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

Adjustments are located on the Power Supply Board. See Programmer Manual.

Confirm Programmer in STOP. Set Programmer in START.

Test Point located on Analog Card.

Confirm Programmer in STOP. Set Programmer in START.

	MODEL 5	9	19	
Load	Bits 2,4,6,8,ON	AA	55	DI Bus
Confirm	Bits 2,4,6,8,ON	55	55	DO Bus
Load	Bits 1,3,5,7,ON	55	AA	DI Bus
Confirm	Bits 1,3,5,7,ON	AA	AA	DO Bus

PROGRAM ABORT

The 701-1225 Digital Control Card contains a programmable counter plus a timer which may be used to cause the programming action to be aborted. pROM U15 is programmed with two different program pulse counts at which these aborts occur. One of the two aborts is selected by jumper JP7. The 'M' position designates military abort while 'C' indicates commercial abort. The actual numbers for these two-abort counts are given in the right-hand side of Drawing 007xxxx contained in the Program Card Manual.

When the program abort point is indicated by a time of program , jumper JP1 is installed. The actual abort time is then determined by adjustment R10. The 007-xxxx drawing contains the information.

If an abort occurs it will cause A and/or B verify lights on the Programmer to be extinguished. The program and interrupt lights are on. To escape from this condition, depress Word Skip or Reset. Word Skip causes the address word to be skipped before programming action is reinitiated. Reset causes all controls and indicators to reset to the programer stop condition.

PROGRAM POLARITY

As indicated in the programmed logic level column of the Comparison Chart, certain pROMs program to a Vol (Low Level) while other pROMs program to a Voh (High Level). Therefore, if data from the same input is first programmed into a Vol pROM, and then programmed into a Voh pROM, the two pROM truth tables would be complemented. To correct for this situation, Normal/Invert switches are available on each Data Input assembly. These switches are shown in Figure 1, Sections F, G, H, and I. With all the Input Polarity switches in the Normal position, the following conditions cause a data bit display to illuminate on the Programmer Panel.

INPUT	INPUT ASSY	FIG
A hole in the paper tape	701-1111	1F
A mark on a Mark Sense Card	701-1111	1F
A Low on the Computer Input Port	701-1112	1F
A Low on the Serial Input Port	701-1190	
A Low on the Read-Only Input	701-1187	1E
A keystroke on the Programmer keyboard		
An ASCII Hex character decode active low	701-1117	1D
An 'L' in the BHLF Translator	701-1138	1C
A 'P' in the BPNF Translator	701-1138	1C

The data bit light always becomes a programmed bit in the pROM. For Vol pROMs, a light indicates a Low. For Voh pROMs, a light indicates a programmed High. If it is determined that a logic inversion exists, simply switch the appropriate input to Invert.

It should be noted that if the program card is used to first read data from a pROM into RAM and then this RAM information is programmed into new pROMs, the polarity is always correct. Also, in the ROM 2 to RAM mode of operation, any program card of the correct configuration may be used to read data into RAM. For example, any manufacturer's 256x4 pROM can be read with any 256x4 program card. However, when programming, the correct program card must be used with each device type to be programmed.

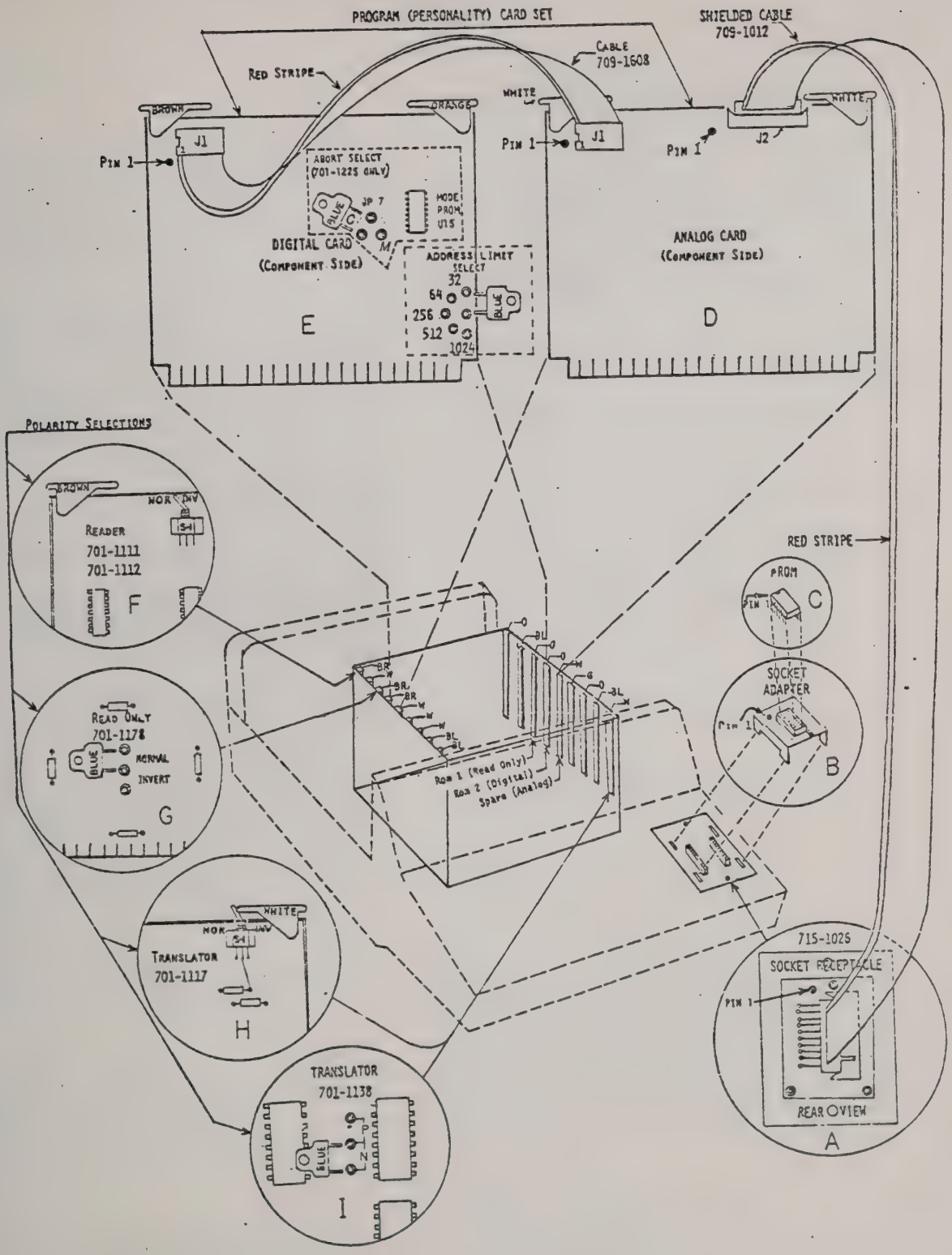

PROGRAM (PERSONALITY) CARD SET
SHIELDED CABLE
709-1012
CABLE
709-1608
RED STRIPE
BROWN
ORANGE
WHITE
PIN 1
J1
J2
ABORT SELECT
(701-1225 ONLY)
JP 7
MODE PROM U15
DIGITAL CARD
(COMPONENT SIDE)
ADDRESS LIMIT SELECT
32
64
256
512
1024
BLUE
E
ANALOG CARD
(COMPONENT SIDE)
D
POLARITY SELECTIONS
NOR
INV
S4
READER
701-1111
701-1112
F
READ ONLY
701-1178
S1
NORMAL
INVERT
G
TRANSLATOR
701-1117
H
TRANSLATOR
701-1138
I
PROM
C
SOCKET ADAPTER
B
Row 1 (Read Only)
Row 2 (Digital)
Spare (Analog)
715-1026
SOCKET RECEPTACLE
REAR VIEW
A

FIGURE 1

UNIVERSAL CALIBRATOR
910-1071

INTRODUCTION

The Universal Calibrator 910-1071 is designed to provide a performance check of Data I/O Program Card Sets in conjunction with a Data I/O PROM Programmer. The performance check includes calibration adjustments of program waveform amplitudes and includes go/no-go tests of all critical programming parameters. Also included in the performance check are tests on resistively loaded ac waveforms.

Since PROM manufacturers' shipments can vary from lot to lot, slight variations in PROM programming yields are to be expected. However, each manufacturer usually specifies certain minimum PROM programming yields—provided that specific approved programming techniques are employed. Data I/O Programmers use manufacturer-approved programming techniques; therefore, if programming yields drop below PROM manufacturers' recommended minimums, or if the program card set has been in use for more than ninety days since its last calibration, programmer performance should be checked.

NECESSARY DOCUMENTATION AND EQUIPMENT

To make performance checks of Data I/O Program Card Sets you will require calibration procedures and charts. Each Program Card Set is provided with a separate calibration and test procedure in its instruction manual.

MODEL 9 USERS NOTE:

Calibration and test procedures supplied with Program Card Sets shipped prior to December 5, 1977 allow calibration with Model 1-5 only. To calibrate using a Model 9, you must have a Program Card Set Manual dated Dec 77 or later, or have an undated calibration procedure and chart with "P9 Update" shown in the revision block of the calibration chart. Updated procedures and charts are available free of charge from the Data I/O factory.

Each Program Card set is also provided with a calibration adapter which plugs into the Universal Calibrator.

MODEL 9 USERS NOTE:

Calibration of the following MOS card sets requires a calibration adapter of revision E or later:

909-1177-1 (NAT 4204/5204)
909-1178-1 (NAT 4203/5203/2)
909-1230-1 (AMI 6834/5204A)
909-1183-1 (1702A)

Revision D or earlier adapters used to calibrate these MOS card sets require modification in order to be used with the Model 9. You'll find the revision letter following the part number (eg. 702-1073X) on the adapter. For further information regarding these card sets, contact your nearest service center.

The following equipment is required for PCS performance check and calibration procedures:

1. Data I/O Universal Calibrator, P/N 910-1071.

2. A. Programmers 1, 2, 3, 5: Data I/O Extender Fixture P/N 910-1136.

   B. Programmer 9: Data I/O Extender Fixture, P/N 910-1074.

3. Digital Voltmeter: Fluke Model 8000A or equivalent.

4. Adjustment Tool: A three inch screwdriver.

5. Dual Trace Oscilloscope: Tektronix 465 or equivalent.

6. Programmers 1, 2, 3, 5 only: Data I/O 13 inch Interconnect Cable, P/N 709-1613.

7. Programmer 9 only: Data I/O Interconnect Cables, P/N 709-1613 and 709-2608

8. Jumper wires approximately 12 inches in length

Installation and calibration procedures are given in each program card set manual.

TECHNICAL DESCRIPTION

Introduction

As shown in Figure 1., the Universal Calibrator interfaces between the Programmer Main Electronics and the Analog Card of the Program Card Set. Essentially, the Universal Calibrator replaces the control functions which are normally performed by the Digital Card during PROM programming. During calibration, the Universal Calibrator provides static control to the Analog Card, allowing up to 24 Analog Card PROM outputs to be individually inspected under DC steady-state conditions.

Calibration Program Adapter

The Calibrator Program Adapter contains a program in ROM which is used to control the Analog Card being checked or calibrated. Addresses arriving from the Programmer are converted into control instructions in the Adapter. These instructions, in turn, are fed through Buffers U1-U4 and enter the Analog Card at J1.

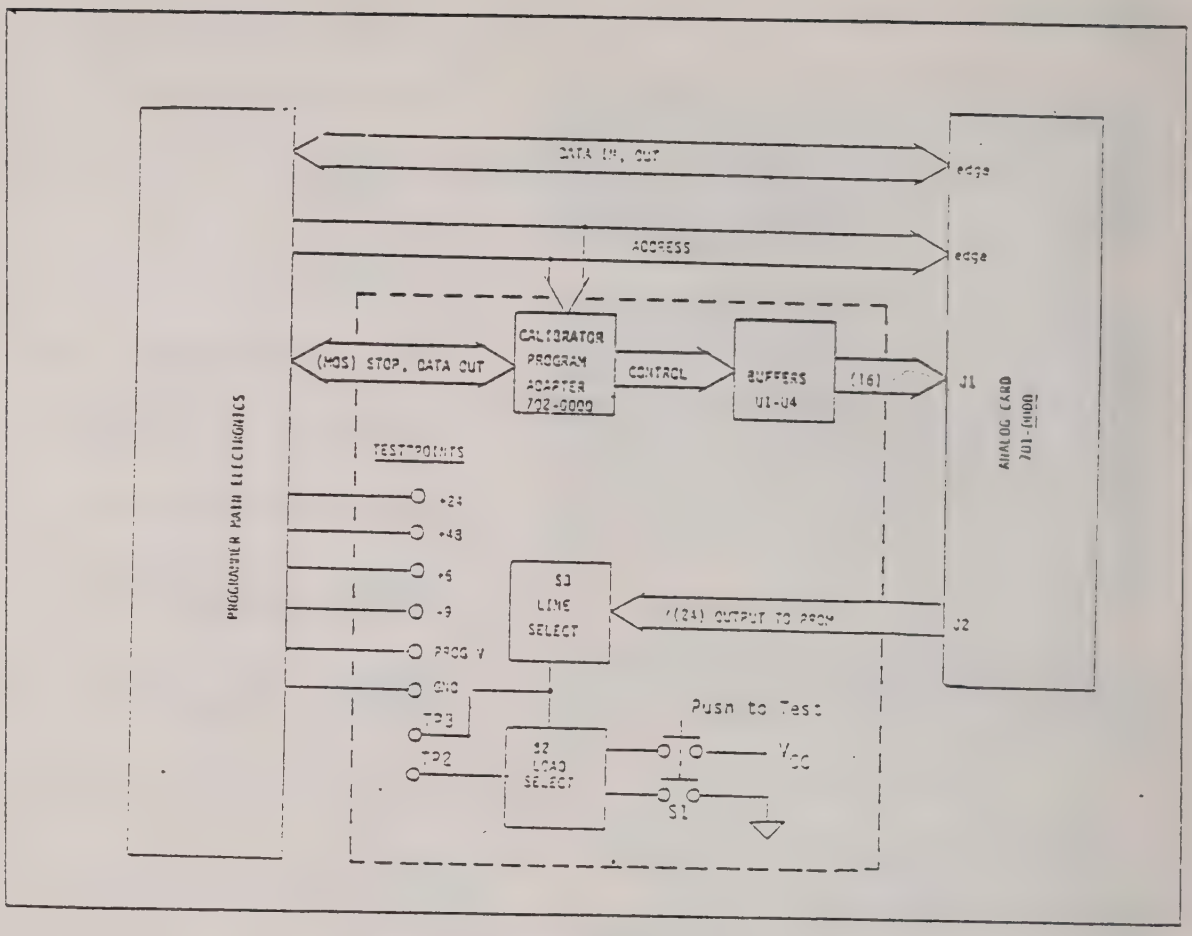


Figure 1. Block Diagram of Universal Calibrator.

Analog Card Output

Output from Analog Card J2 is routed through Line Select switch S3 and to Load Select Switch S2. S3 selects one of the 24 Analog Card PROM outputs. S2 is used to select various resistive loads. S1 is 'push to test' and used to connect the high current load resistors in S2 to ground or VCC when taking DVM readings.

DATA I/O FIELD SERVICES

Data I/O Corp. furnishes complete programmer repair and calibration services at regional Field Service Centers and at the Data I/O factory. Contact your local Data I/O representative for further information.

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O/s option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

Shipment

Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

All products returned to Data I/O must be sent prepaid F.O.B. The warranty is voided if returned items are not packaged by the customer in original packing material, or in other Data I/O approved containers. If reshipment method is not specified by customer, Data I/O will return products by most expedient shipping method, F.O.B. our plant.

Ship returned equipment to:

DATA I/O CORPORATION
1297 N.W. Mall
Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

Parts Ordering

Orders for parts should contain the following information:

a. Description of part(s) and Data I/O part number(s).
b. Quantity of each item to be ordered.
c. Equipment serial number and model number.
d. Corporate name of firm.
e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
h. Billing information.
i. Purchase order number.
j. Method of shipment.

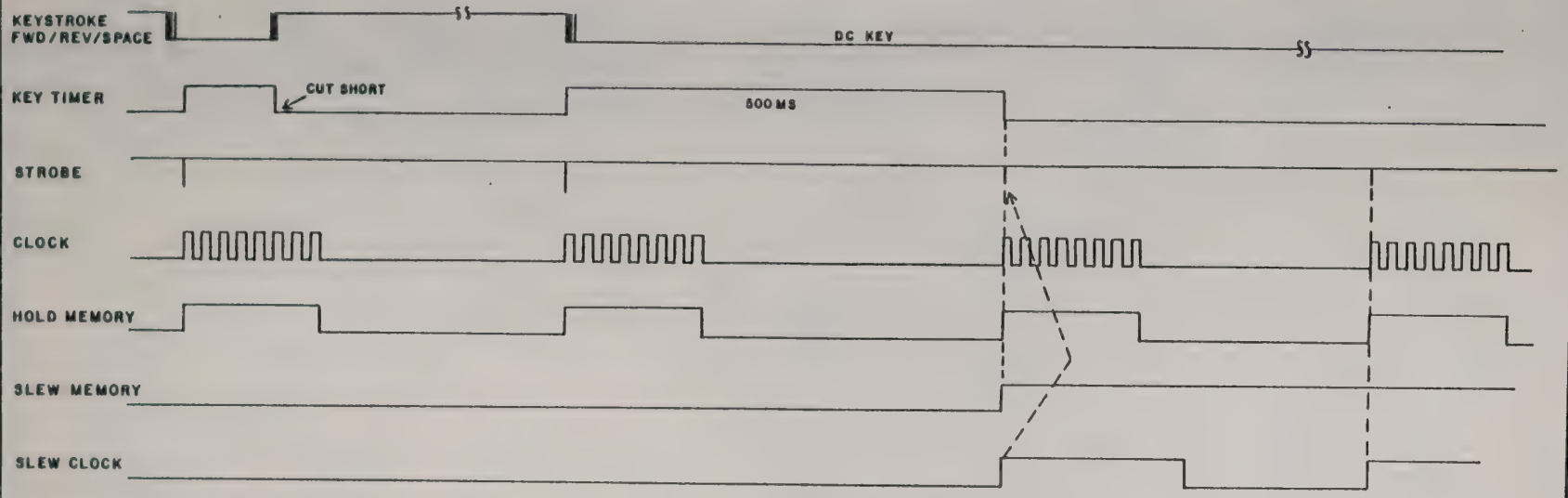
Please send all parts orders to:

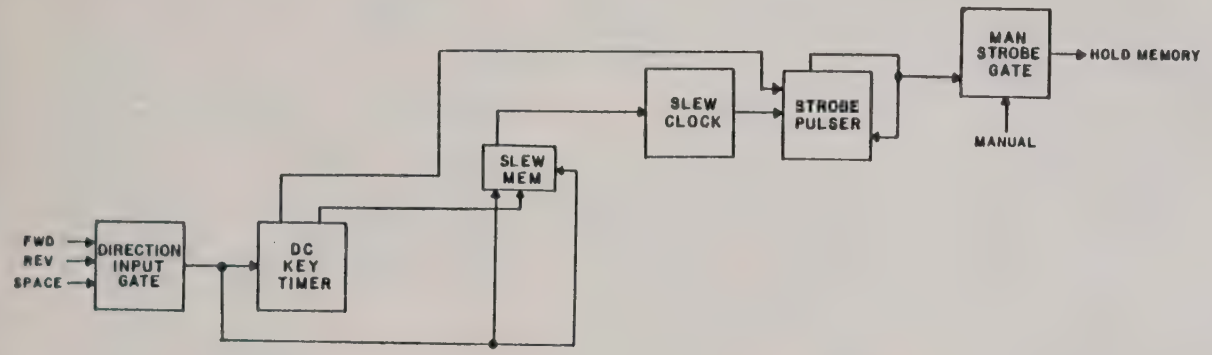
DATA I/O CORPORATION
P O Box 308
Issaquah, Washington 98027

From Europe:

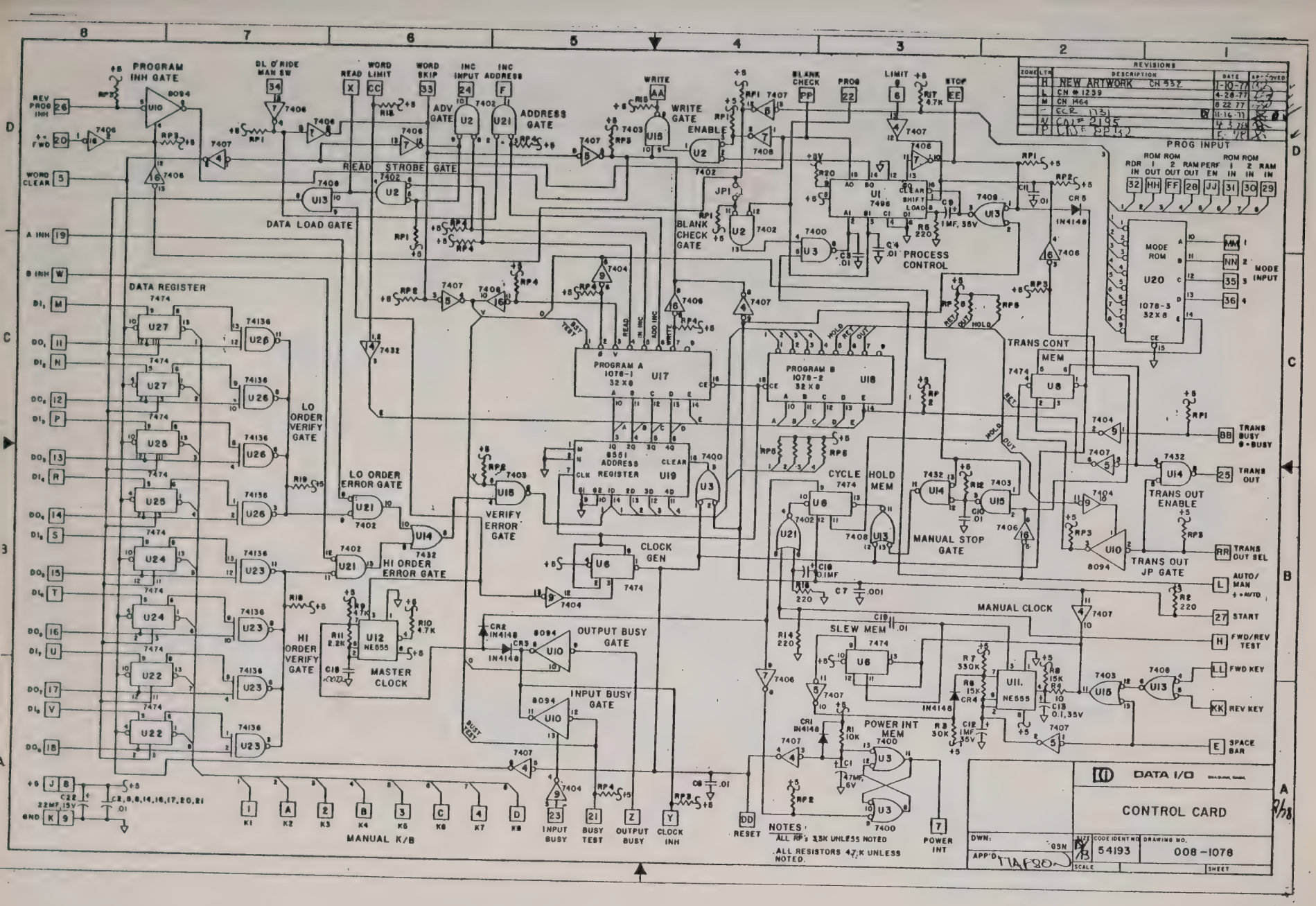
DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

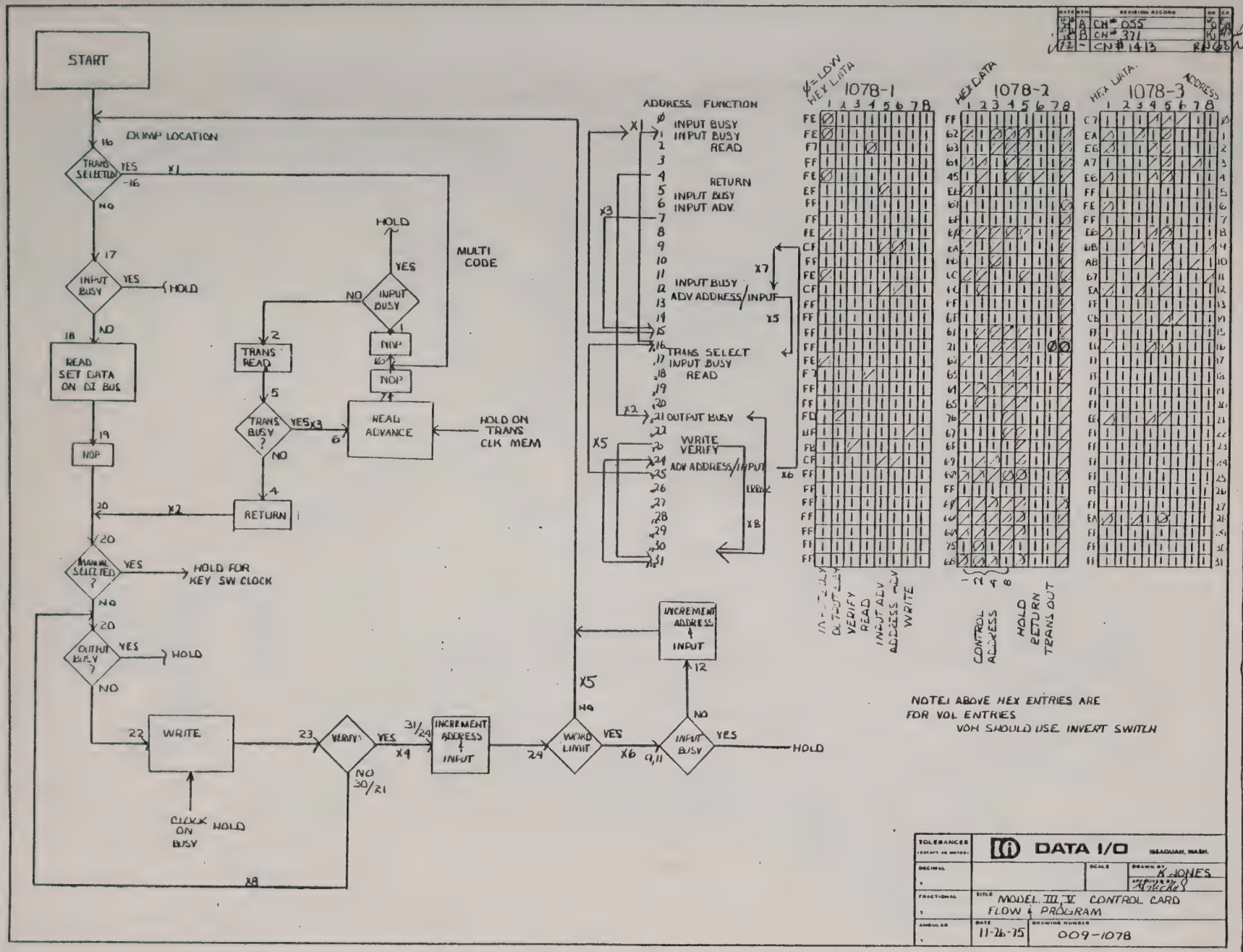
REVISION RECORD					
DATE	BY			DR	CK
7/A	A	RELEASE			





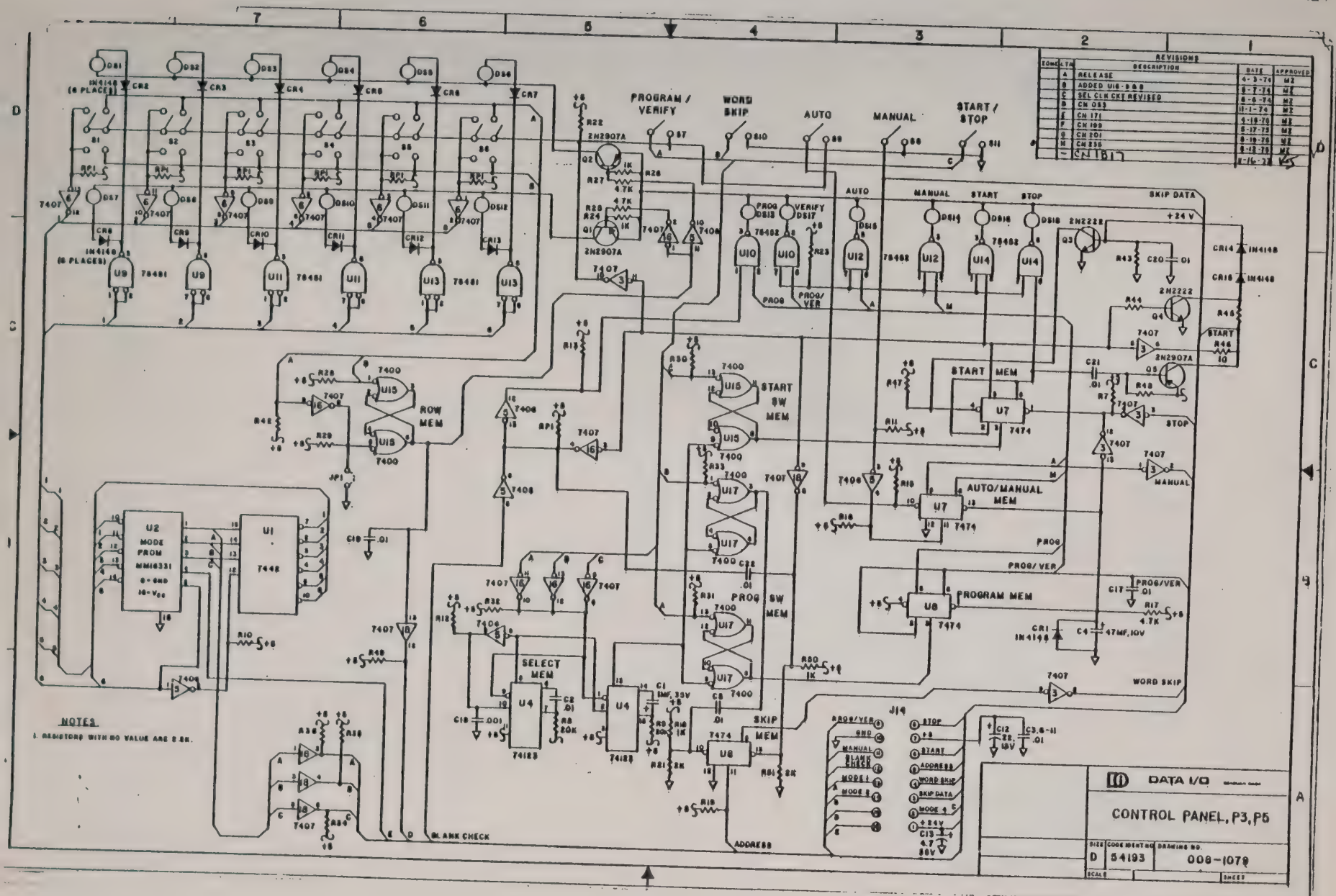
TOLERANCES (EXCEPT AS NOTED)	DATA I/O REDMOND, WASH.		
DECIMAL .	BLOCK & TIMING DIAGRAM	SCALE	DESIGN BY W. QUILLIN
FRACTIONAL 1	TITLE CONTROL CARD STEP & SLEW CONTROL		APPROVED BY
ANGULAR .	DATE 12-10-73	DRAWING NUMBER 007-1078	

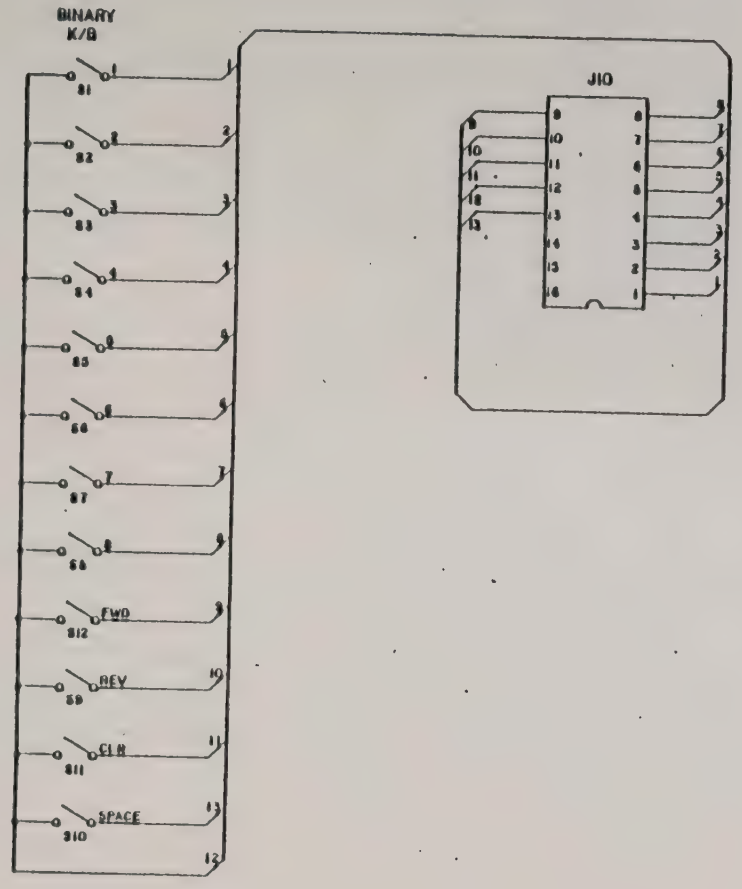

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
H NEW ARTWORK CN 532 1-10-77
L CN # 1239 4-28-77
M CN M64 8 22 77
- ECR 1131 11-16-77
N CAL # 2195 4 3 78
P CAL # 2212 5 1 78
PROGRAM INH GATE
DL O'RIDE MAN SW
READ
WORD LIMIT
WORD SKIP
INC INPUT
INC ADDRESS
WRITE
BLANK CHECK
PROG
LIMIT
STOP
ADV GATE
ADDRESS GATE
WRITE GATE ENABLE
READ STROBE GATE
DATA LOAD GATE
BLANK CHECK GATE
PROCESS CONTROL
PROG INPUT
ROM ROM ROM ROM
RDR I 2 RAM PERF I Z RAM
IN OUT OUT OUT EN IN IN IN
MODE ROM U20 1078-3 32X8
MODE INPUT
DATA REGISTER
LO ORDER VERIFY GATE
LO ORDER ERROR GATE
HI ORDER ERROR GATE
HI ORDER VERIFY GATE
MASTER CLOCK
VERIFY ERROR GATE
CLOCK GEN
OUTPUT BUSY GATE
INPUT BUSY GATE
PROGRAM A 1078-1 32X8 U17
PROGRAM B 1078-2 32X8 U18
8551 ADDRESS REGISTER U19
TRANS CONT MEM
CYCLE HOLD MEM
MANUAL STOP GATE
TRANS OUT ENABLE
TRANS OUT JP GATE
MANUAL CLOCK
SLEW MEM
POWER INT MEM
REV PROG INH
FWD
WORD CLEAR
A INH
B INH
DI1 M
DO1 11
DI2 N
DO2 12
DI3 P
DO3 13
DI4 R
DO4 14
DI5 S
DO5 15
DI6 T
DO6 16
DI7 U
DO7 17
DI8 V
DO8 18
GND K 9
MANUAL K/B
1 A 2 B 3 C 4 D
K1 K2 K3 K4 K5 K6 K7 K8
INPUT BUSY
BUSY TEST
OUTPUT BUSY
CLOCK INH
DD RESET
POWER INT
BB TRANS BUSY 0=BUSY
25 TRANS OUT
RR TRANS OUT SEL
L AUTO/MAN +=AUTO
27 START
H FWD/REV TEST
LL FWD KEY
KK REV KEY
E SPACE BAR
NOTES:
ALL RP's 33K UNLESS NOTED
ALL RESISTORS 47K UNLESS NOTED.
DATA I/O
CONTROL CARD
DWN: GSN
APP'D TIA 2-80
SIZE B
CODE IDENT NO 54193
DRAWING NO. 008-1078
SCALE
SHEET



REVISION RECORD			
A	CN# 055		
B	CN# 371		
-	CN# 1413		

TOLERANCES (UNLESS AS NOTED)	DATA I/O REDMOND, WASH.
DECIMAL	SCALE
FRACTIONAL	DRAWN BY K. JONES
ANGULAR	TITLE MODEL III, V CONTROL CARD FLOW & PROGRAM
	DATE 11-26-75
	DRAWING NUMBER 009-1078


REVISIONS
DESCRIPTION
DATE
APPROVED
A RELEASE 4-3-74 MZ
B ADDED U16-D&E 5-7-74 MZ
C SEL CLK CKT REVISED 6-6-74 MZ
D CN 053 11-1-74 MZ
E CN 171 5-15-75 MZ
F CN 199 8-17-75 MZ
G CN 201 8-19-76 MZ
H CN 236 9-12-78 MZ
J CN 317 11-16-78 MZ
PROGRAM / VERIFY
WORD SKIP
AUTO
MANUAL
START / STOP
SKIP DATA
+24 V
START MEM
STOP
MANUAL
AUTO/MANUAL MEM
PROG
PROG/VER
PROGRAM MEM
WORD SKIP
ROW MEM
START SW MEM
PROG SW MEM
SELECT MEM
SKIP MEM
ADDRESS
BLANK CHECK
MODE FROM MMI6331
NOTES
1. RESISTORS WITH NO VALUE ARE 2.2K.
DATA I/O
CONTROL PANEL, P3, P5
SIZE D
CODE IDENT NO 54193
DRAWING NO. 008-1079
SCALE
SHEET



RELEASE

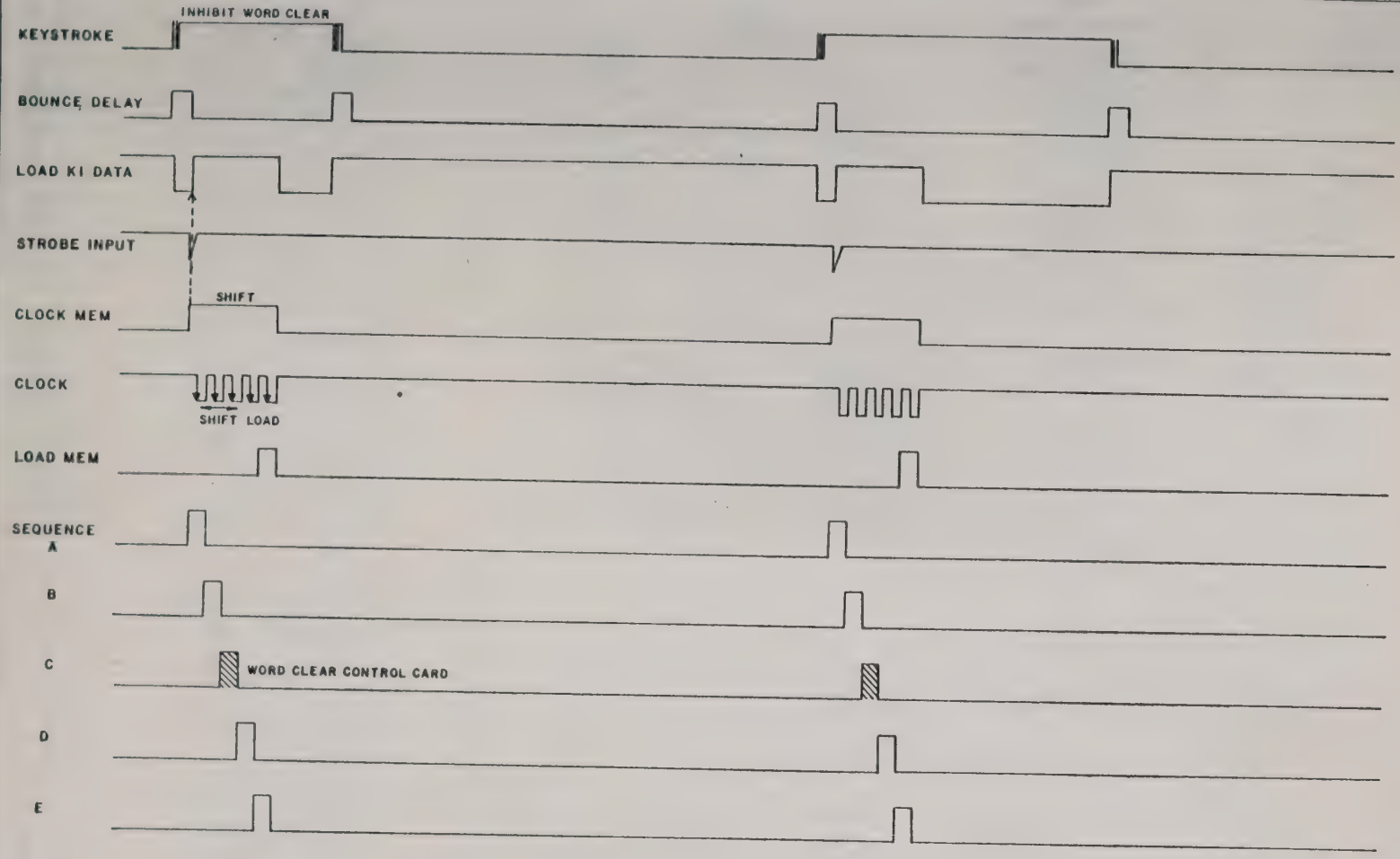
DATA I/O

BINARY K/B

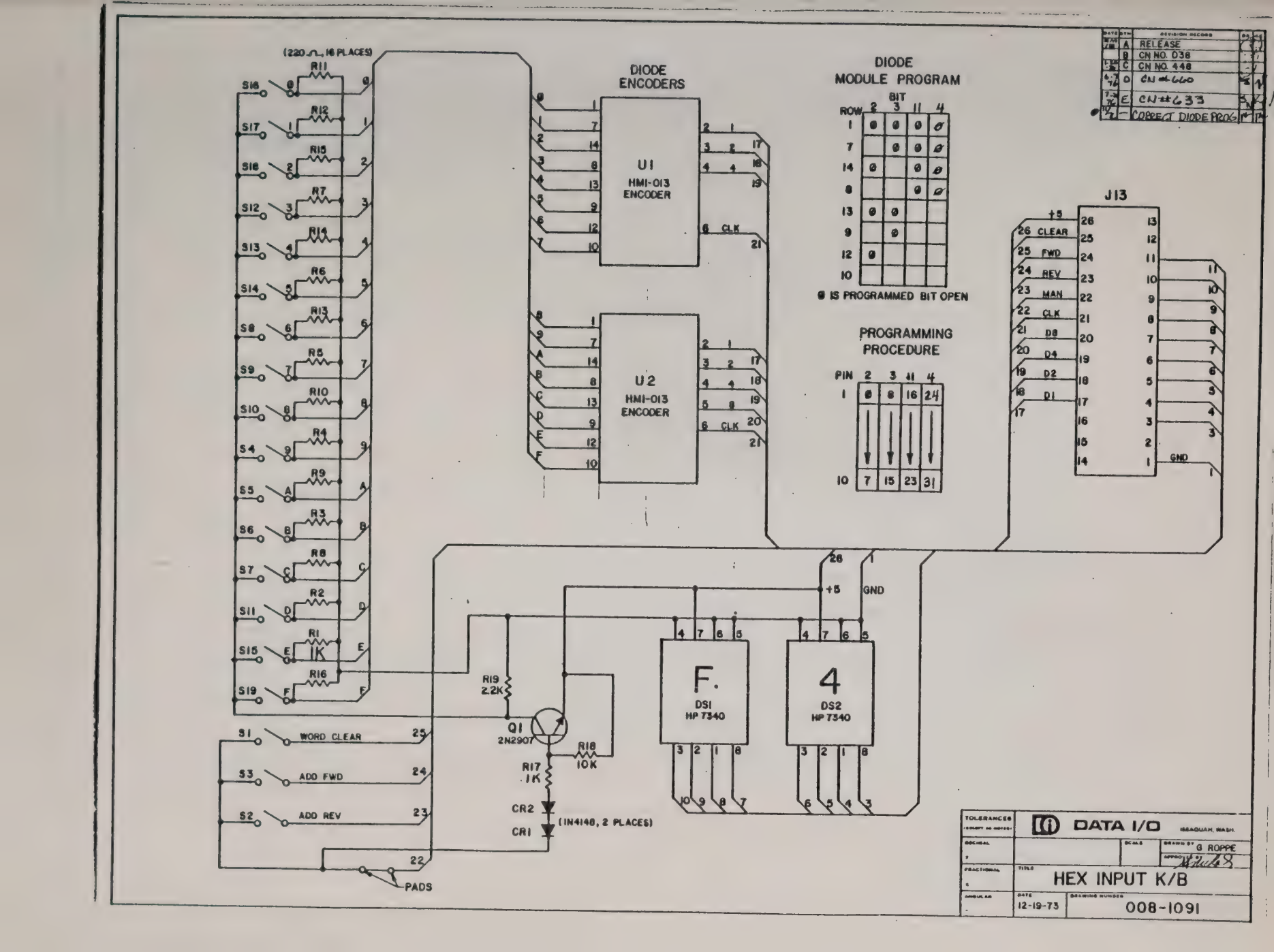
12-19-73

008-1090

DATE	BY	REVISION RECORD	DR	CK
4/24	RJ	RELEASE		



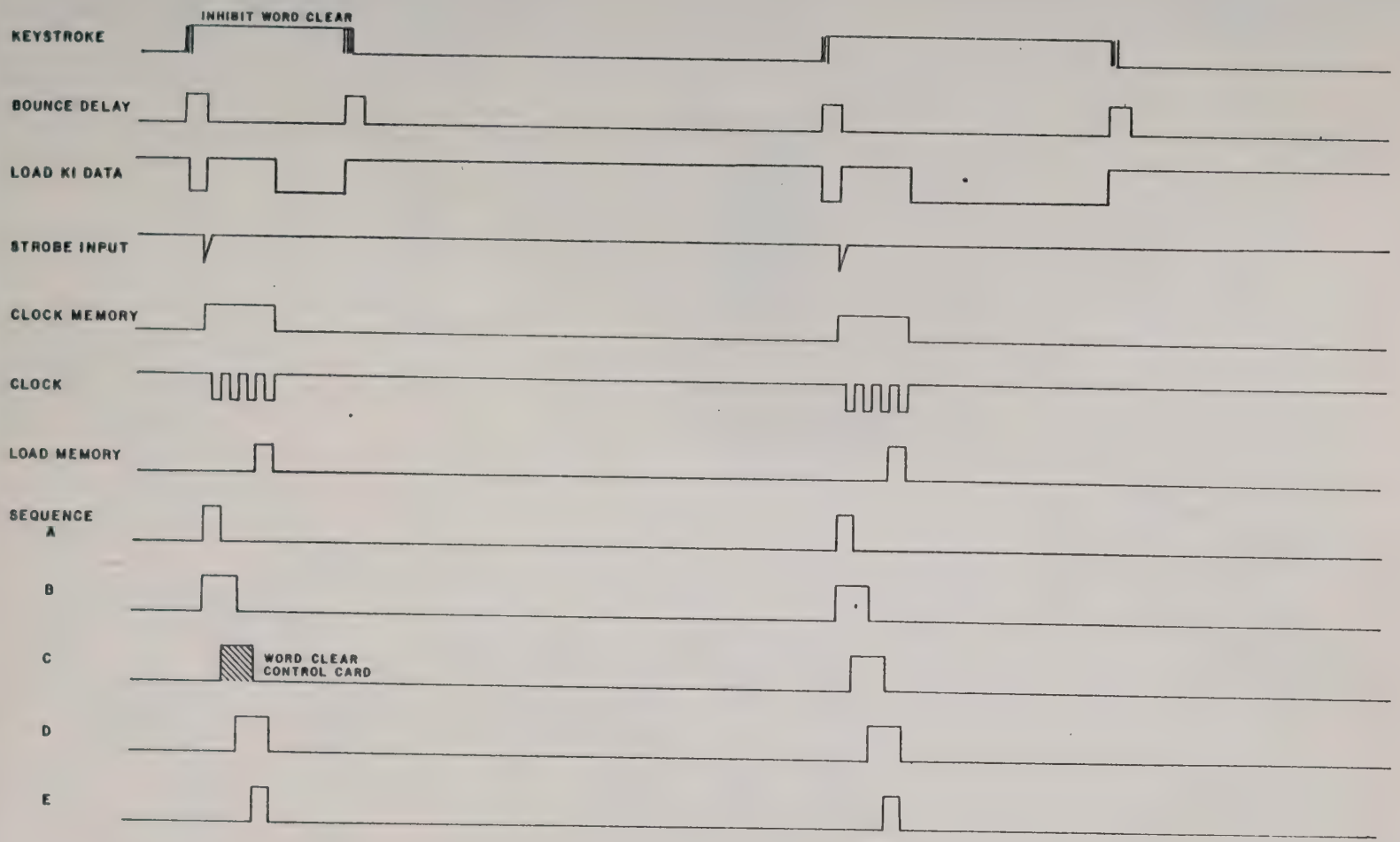
TOLERANCES (EXCEPT AS NOTED)	DATA I/O REDMOND, WASH.		
DECIMAL .	TIMING DIAGRAM	SCALE	DRAWN BY K JONES
FRACTIONAL .	TITLE HEX KEYBOARD		
ANGULAR .	DATE 6-4-73	DRAWING NUMBER 007-1091	



DATE	DTR	REVISION RECORD
8/20/73	A	RELEASE
9/28/73	B	CN NO. 038
11/28/73	C	CN NO. 448
6/7/74	D	CN #660
7-30-74	E	CN #633
12/4/74	—	CORRECT DIODE PROG

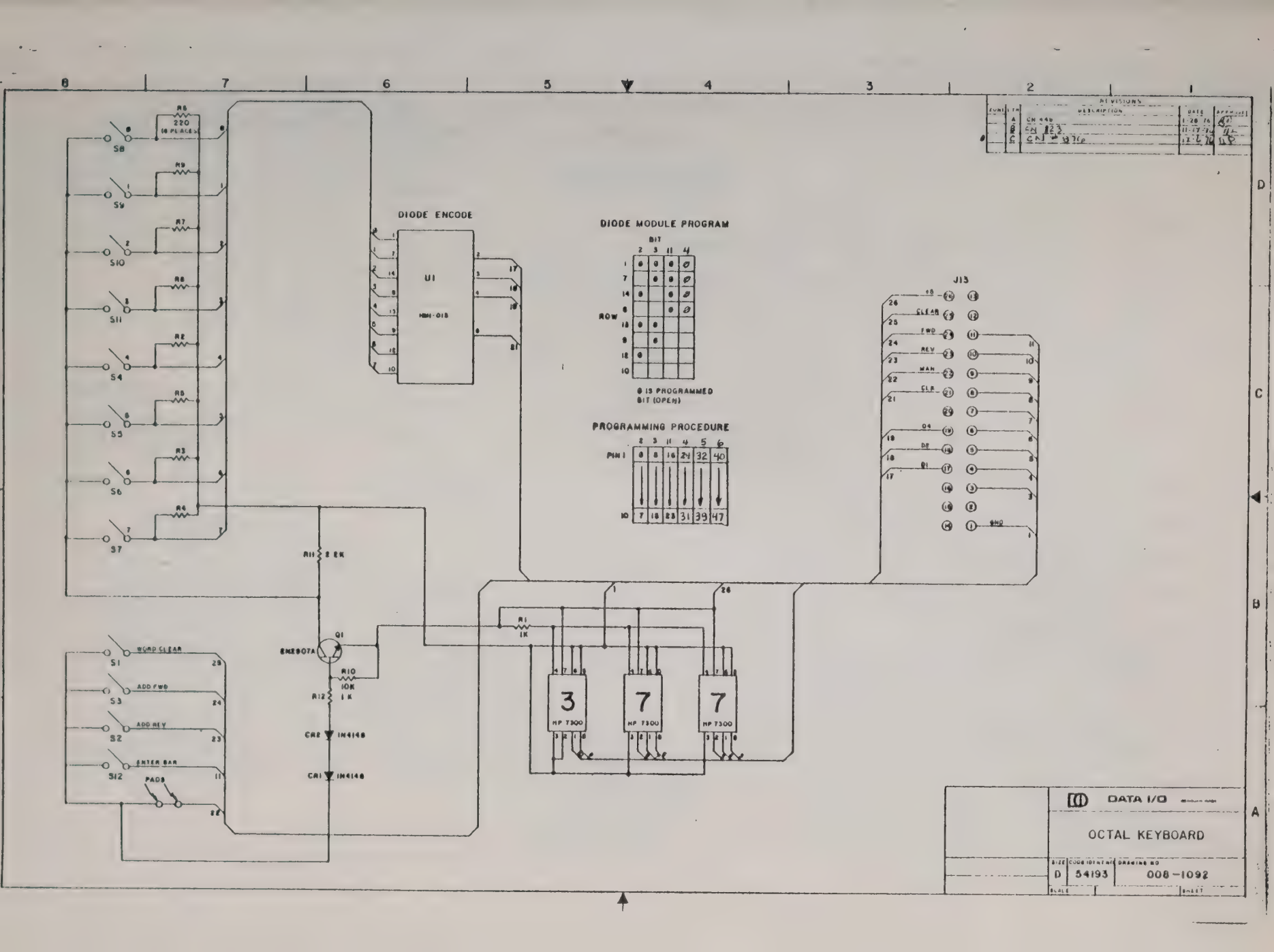
TOLERANCES (UNLESS OTHERWISE NOTED)	DATA I/O REDMOND, WASH.	
DECIMAL .	SCALE	DRAWN BY G ROPPE
FRACTIONAL 1/	TITLE	HEX INPUT K/B
ANGULAR .	DATE 12-19-73	DRAWING NUMBER 008-1091

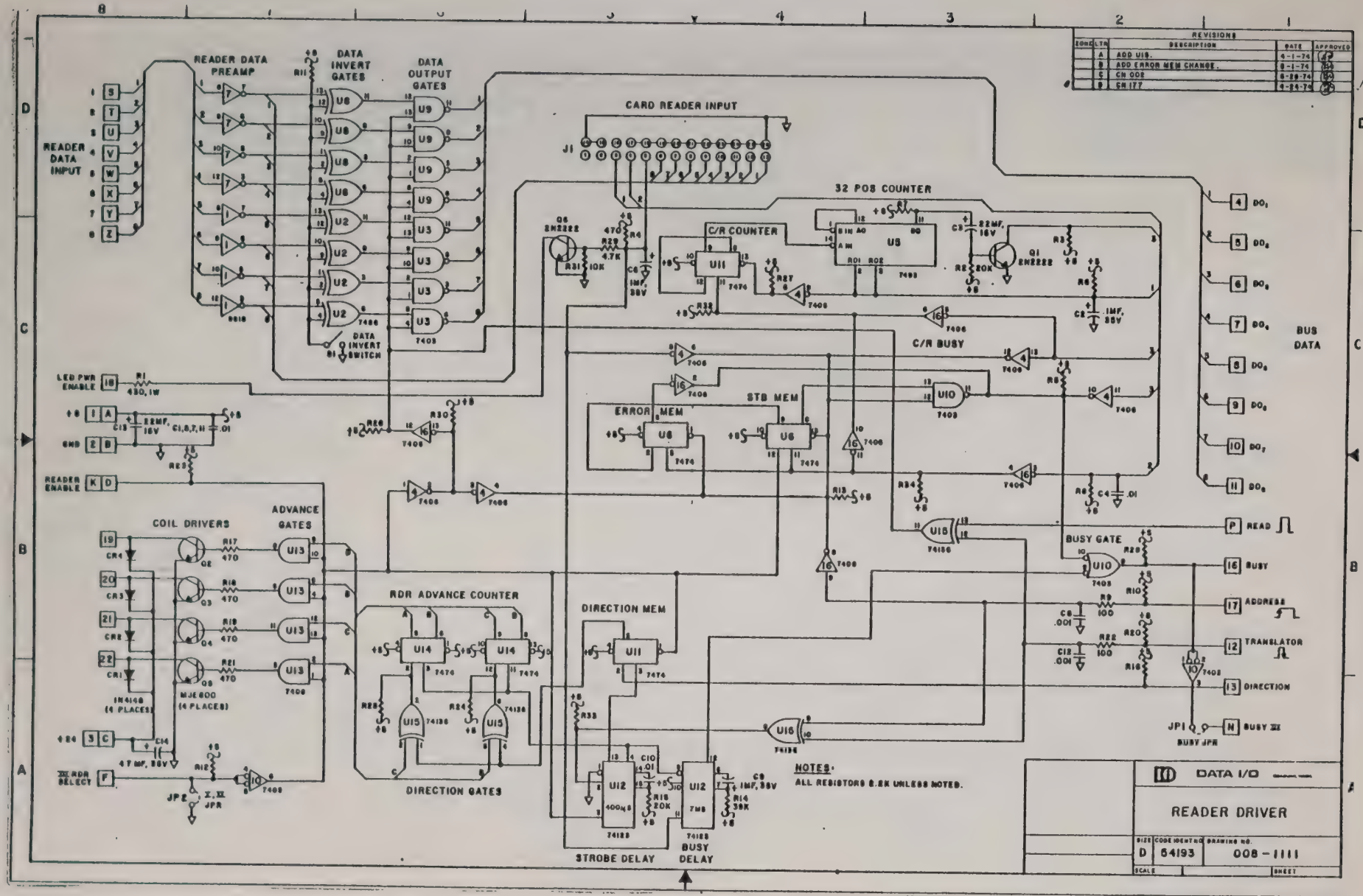
DATE	BY	REVISION RECORD	DR	CK
7/1	A	RELEASE		

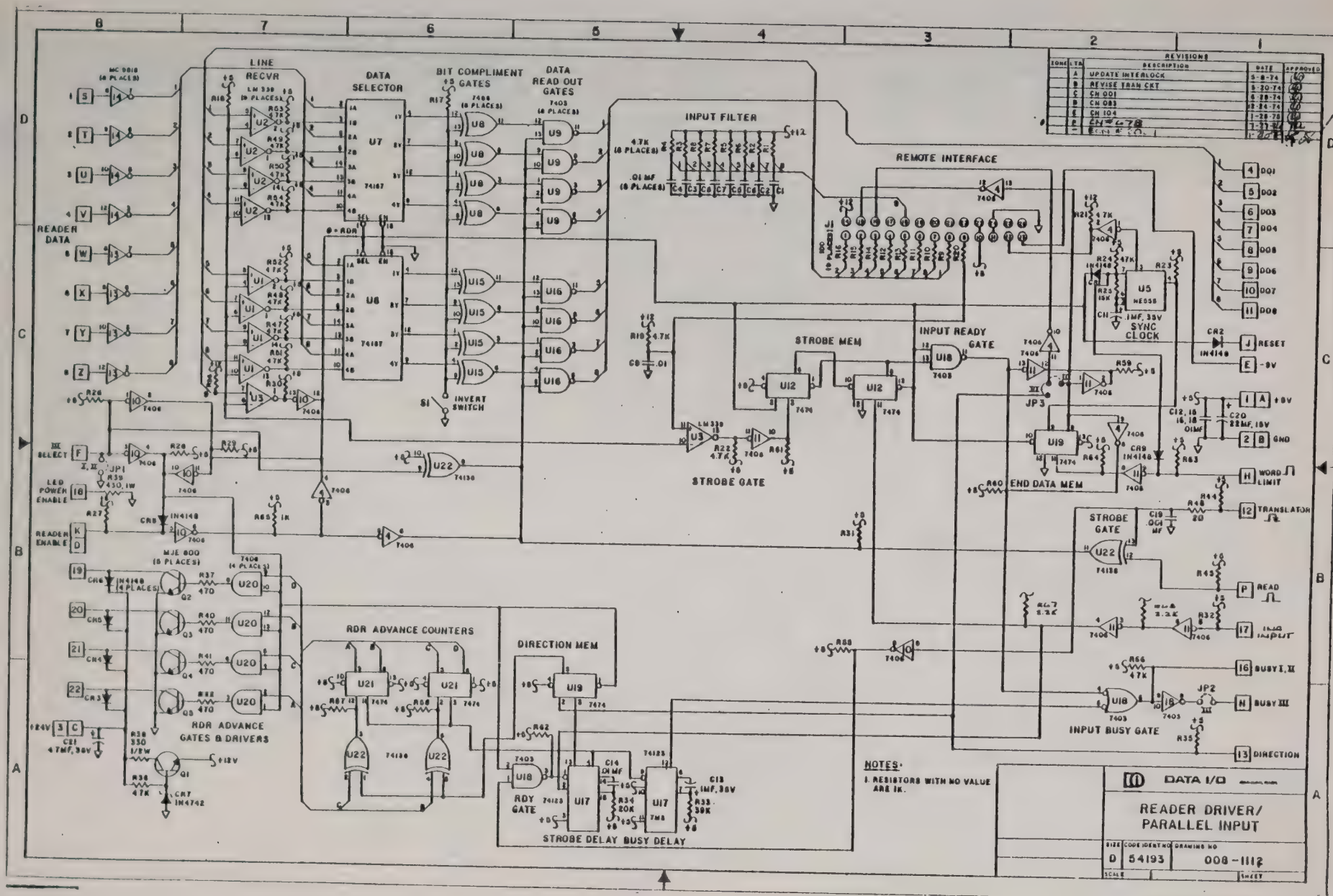


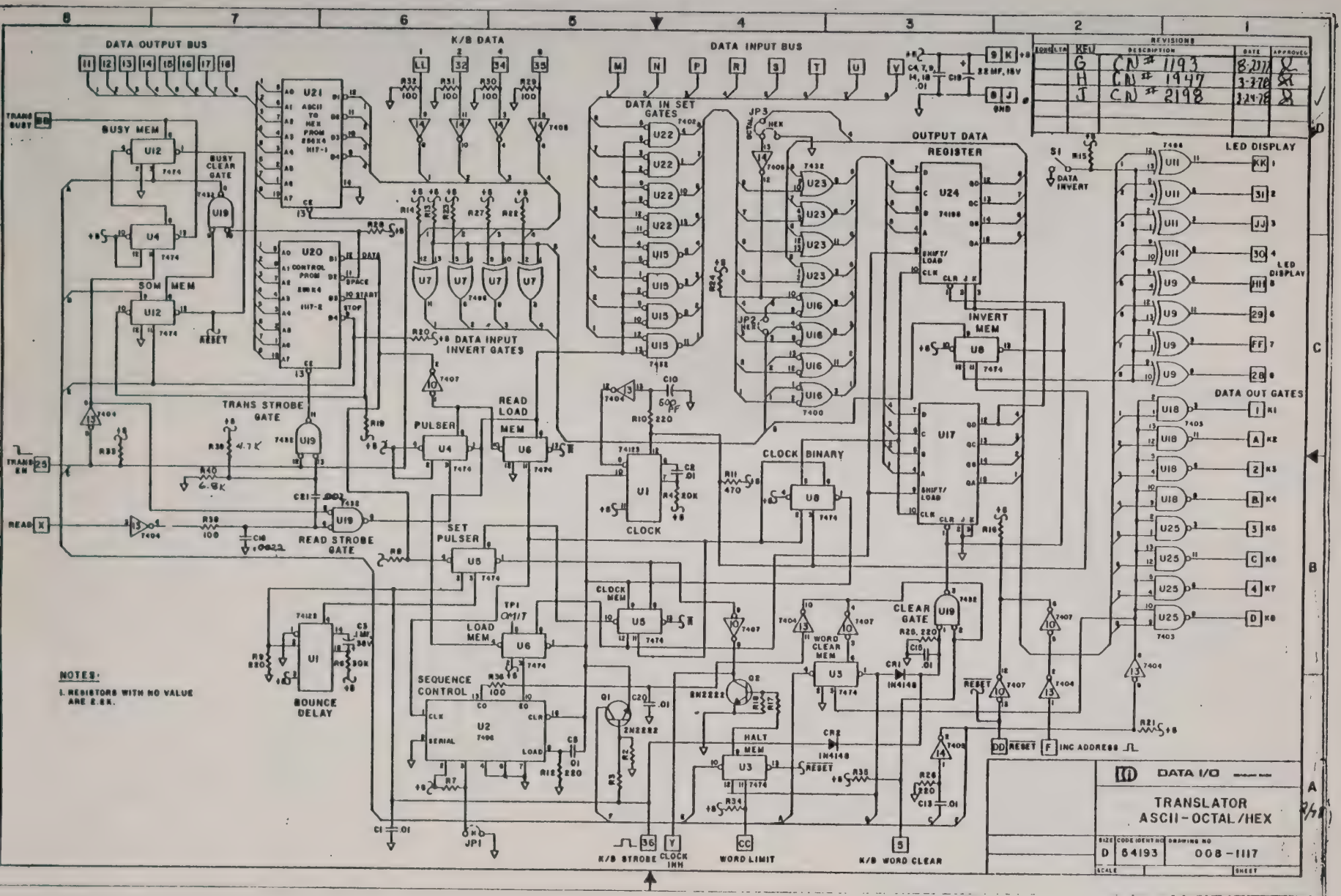
TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL .	TIMING DIAGRAM	SCALE	DRAWN BY K. JONES
FRACTIONAL .	TITLE OCTAL KEYBOARD		
ANGULAR .	DATE 6-4-74	DRAWING NUMBER 007-1092	

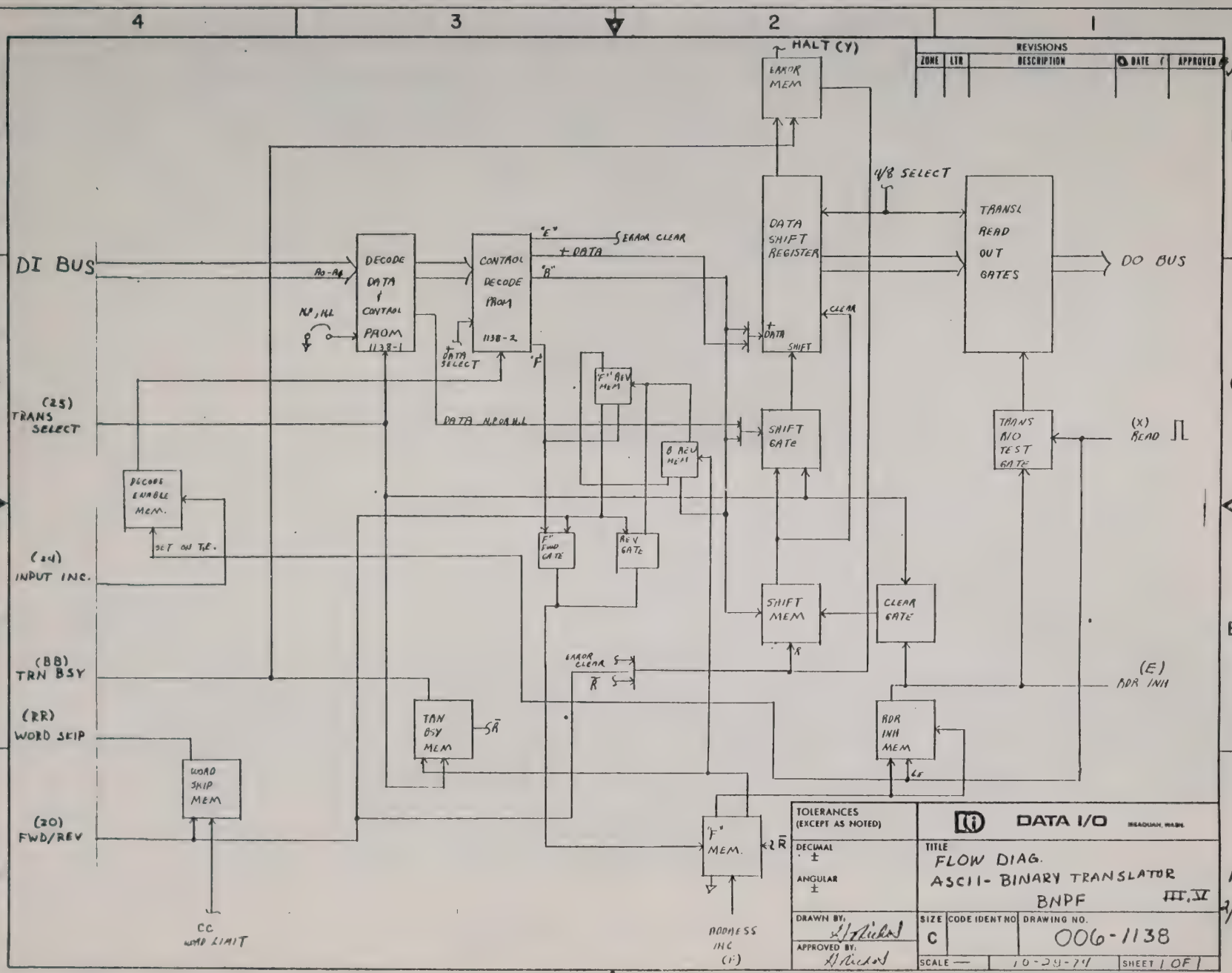
2/8

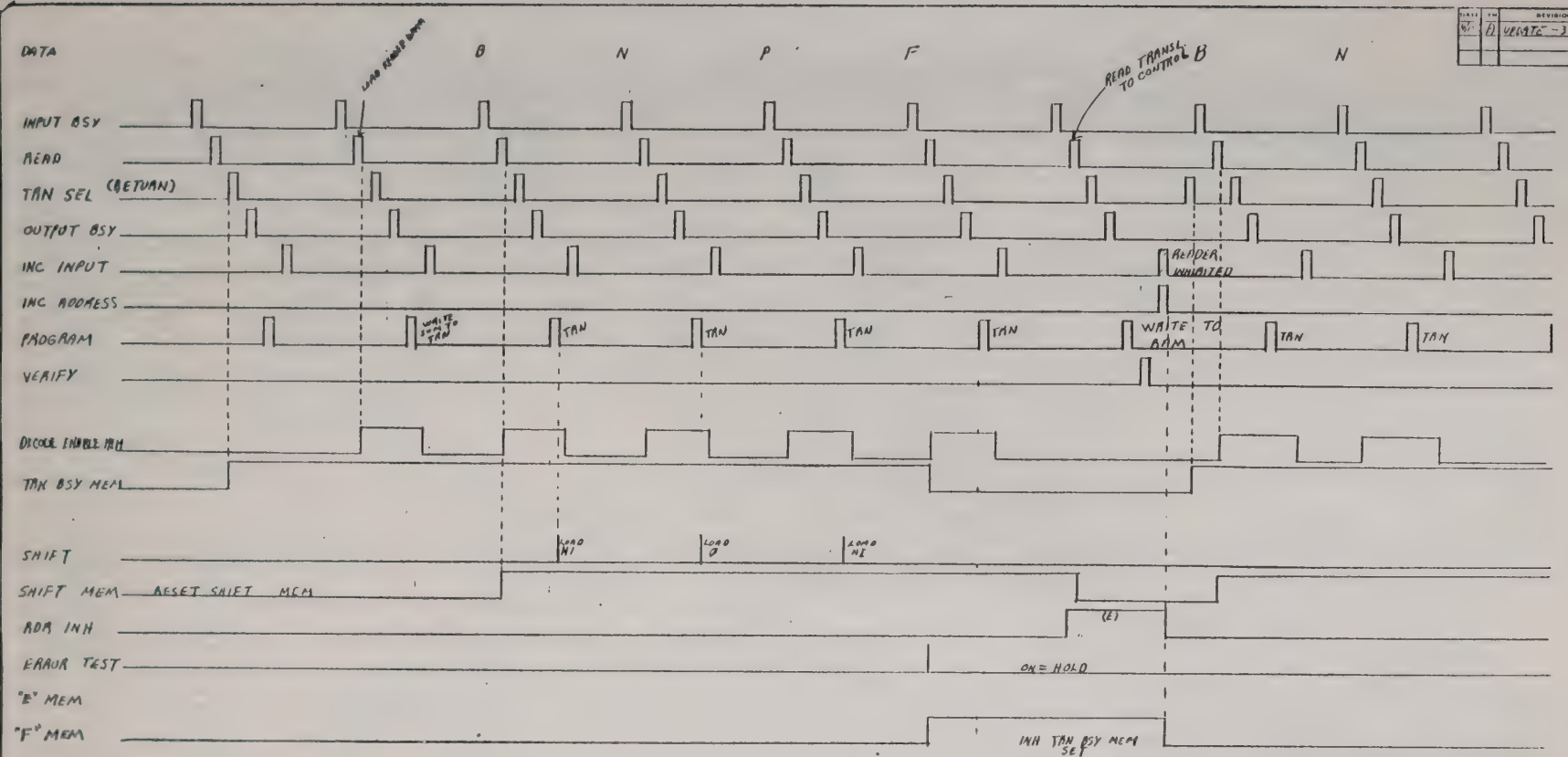

DIODE ENCODE
U1
MM-018
DIODE MODULE PROGRAM
BIT
2 3 11 4
ROW
1
7
14
6
18
9
12
10
0 IS PROGRAMMED
BIT (OPEN)
PROGRAMMING PROCEDURE
PIN 1
2 3 11 4 5 6
0 0 16 24 32 40
10
7 15 23 31 39 47
J13
CLEAR
FWD
REV
MAN
CLR
D4
D2
D1
GND
R5
220
(8 PLACES)
S8
S9
S10
S11
S4
S5
S6
S7
R11 2 EK
Q1
2N3904
R10
10K
R12
1K
CR2 IN4148
CR1 IN4148
R1
1K
WORD CLEAR
S1
ADD FWD
S3
ADD REV
S2
ENTER BAR
S12
PADS
3
7
7
MP 7300
REVISIONS
DESCRIPTION
DATE
APPROVED
DATA I/O
OCTAL KEYBOARD
SIZE
D
CODE IDENT NO
54193
DRAWING NO
008-1092
SCALE
SHEET


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A ADD U16. 4-1-74
B ADD ERROR MEM CHANGE. 5-1-74
C CN 008 6-28-74
D CN 177 9-24-74
READER DATA INPUT
READER DATA PREAMP
DATA INVERT GATES
DATA OUTPUT GATES
DATA INVERT SWITCH
CARD READER INPUT
J1
32 POS COUNTER
C/R COUNTER
C/R BUSY
ERROR MEM
STB MEM
BUS DATA
LED PWR ENABLE
READER ENABLE
COIL DRIVERS
ADVANCE GATES
IN4148 (4 PLACES)
MJE800 (4 PLACES)
RDR ADVANCE COUNTER
DIRECTION GATES
DIRECTION MEM
BUSY GATE
STROBE DELAY
BUSY DELAY
READ
BUSY
ADDRESS
TRANSLATOR
DIRECTION
BUSY JPR
NOTES:
ALL RESISTORS 0.5K UNLESS NOTED.
DATA I/O
READER DRIVER
SIZE D
CODE IDENT NO. 64193
DRAWING NO. 008-1111
SCALE
SHEET


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | UPDATE INTERLOCK | 3-8-74
B | REVISE TRAN CKT | 3-20-74
C | CN 001 | 4-18-74
D | CN 003 | 4-24-74
E | CN 104 | 7-28-74
F | CN #478 | 7-31-74
READER DATA
LINE RECVR
DATA SELECTOR
BIT COMPLIMENT GATES
DATA READ OUT GATES
INPUT FILTER
REMOTE INTERFACE
SYNC CLOCK
INPUT READY GATE
STROBE MEM
STROBE GATE
END DATA MEM
INPUT BUSY GATE
RDR ADVANCE COUNTERS
RDR ADVANCE GATES & DRIVERS
DIRECTION MEM
RDY GATE
STROBE DELAY BUSY DELAY
INVERT SWITCH
LED POWER ENABLE
READER ENABLE
SELECT
RESET
-9V
+8V
GND
WORD LIMIT
TRANSLATOR
READ
BUSY I, II
BUSY III
DIRECTION
NOTES:
1. RESISTORS WITH NO VALUE ARE 1K.
DATA I/O
READER DRIVER/ PARALLEL INPUT
SIZE D
CODE IDENT NO 54193
DRAWING NO 008-1113
SCALE
SHEET


DATA OUTPUT BUS
K/B DATA
DATA INPUT BUS
BUSY MEM
BUSY CLEAR GATE
SOM MEM
RESET
TRANS BUSY 26
TRANS EN 25
READ X
U21 ASCII TO HEX FROM 8566X MIT-1
U20 CONTROL PROM 8MK4 1117-2
DATA
SPACE
START
STOP
+8 DATA INPUT INVERT GATES
DATA IN SET GATES
JP3
HEX
OCTAL
OUTPUT DATA REGISTER
U24 74198
SHIFT/ LOAD
CLR J K
S1
DATA INVERT
LED DISPLAY
INVERT MEM
U8
U17
DATA OUT GATES
TRANS STROBE GATE
PULSER
READ LOAD MEM
U4
U6
U1 CLOCK
CLOCK BINARY
U8
READ STROBE GATE
SET PULSER
U5
CLOCK MEM
LOAD MEM
TP1 OMIT
CLEAR GATE
U19
WORD CLEAR MEM
U3
IN4148
RESET
INC ADDRESS
BOUNCE DELAY
SEQUENCE CONTROL
U2 7496
Q1 2N2222
Q2 2N2222
HALT MEM
K/B STROBE
CLOCK INH
WORD LIMIT
K/B WORD CLEAR
NOTES:
1. RESISTORS WITH NO VALUE ARE 2.8K.
DATA I/O
TRANSLATOR ASCII-OCTAL/HEX
SIZE D
CODE IDENT NO 54193
DRAWING NO 008-1117
SCALE
SHEET
REVISIONS
LTR
KEY
DESCRIPTION
DATE
APPROVED
G CN # 1193 8-2077
H CN # 1947 3-378
J CN # 2198 3-24-78


4
3
2
1
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
HALT (Y)
ERROR MEM
DI BUS
DECODE DATA & CONTROL PROM 1138-1
CONTROL DECODE PROM 1138-2
"E"
ERROR CLEAR
± DATA
"B"
"F"
DATA SELECT
N.P., N.L.
A0-A9
DATA SHIFT REGISTER
+DATA
SHIFT
CLEAR
Ψ8 SELECT
TRANSL READ OUT GATES
DO BUS
(25) TRANS SELECT
DATA N.P.OR N.L.
F' REV MEM
B REV MEM
SHIFT GATE
TRANS NO TEST GATE
(X) READ
DECODE ENABLE MEM.
SET ON T.E.
(24) INPUT INC.
F' FWD GATE
REV GATE
SHIFT MEM
CLEAR GATE
(BB) TRN BSY
ERROR CLEAR S
R S
(E) ADR INH
(RR) WORD SKIP
TAN BSY MEM
SR̄
ADR INH MEM
WORD SKIP MEM
(20) FWD/REV
"F" MEM.
2R̄
CC WORD LIMIT
ADDRESS INC (F)
TOLERANCES (EXCEPT AS NOTED)
DECIMAL ±
ANGULAR ±
DRAWN BY: J. Richard
APPROVED BY: J. Richard
DATA I/O REDMOND, WASH.
TITLE
FLOW DIAG.
ASCII- BINARY TRANSLATOR
BNPF III, V
SIZE C
CODE IDENT NO
DRAWING NO. 006-1138
SCALE —
10-29-74
SHEET 1 OF
4/78



DASH NO.	TM	REVISION RECORD	DR	CK
Ø	D	UPDATE -3 CN 731		

1138-1 PROGRAM U17 P/T

INPUT CHARACTER	DECIMAL ADDRESS	INPUT WORD	OUTPUT DATA "4" 9	"3" 10	"2" 11	"1" 12
B	61, 189	2,7	1	Ø	Ø	1
N	49	2,3,7	Ø	1	Ø	Ø
P	47	5,7	Ø	Ø	Ø	Ø
H	183	4,7	Ø	Ø	Ø	Ø
L	179	3,4,7	Ø	1	Ø	Ø
F	67, 185	2,3,7	1	Ø	1	1
E	58, 186	1,3,7	Ø	Ø	1	1
EOM	124, 252	1,2	Ø	1	1	1
NULL	Ø, 128		1	1	Ø	1
DELETE	127, 255	1-7	1	1	Ø	1

BASIC PN FORMAT

Ø = L
1 = H

1138-2 U12

	DATA BIT TO IRO 6																														
8	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
7	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø	Ø
6	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	Ø
5	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	Ø	1
4	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1
3	1	1	1	1	Ø	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1
2	Ø	1	1	1	1	1	1	1	1	1	Ø	1	1	1	1	1	Ø	1	1	1	1	1	1	1	1	1	Ø	1	1	1	1
1	1	Ø	1	1	1	1	1	1	1	Ø	1	1	1	1	1	1	Ø	1	1	1	1	1	1	Ø	1	1	1	1	1	1	1
ADDRESS	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	P.H	B	N.L		E	F	EOM	—	P.H	B	N.L		E	F	EOM	—	P.H	B	N.L		E	F	EOM	—	P.H	B	N.L		E	F	EOM	—

+DATA = P
+DATA = N
+DATA = H
+DATA = L

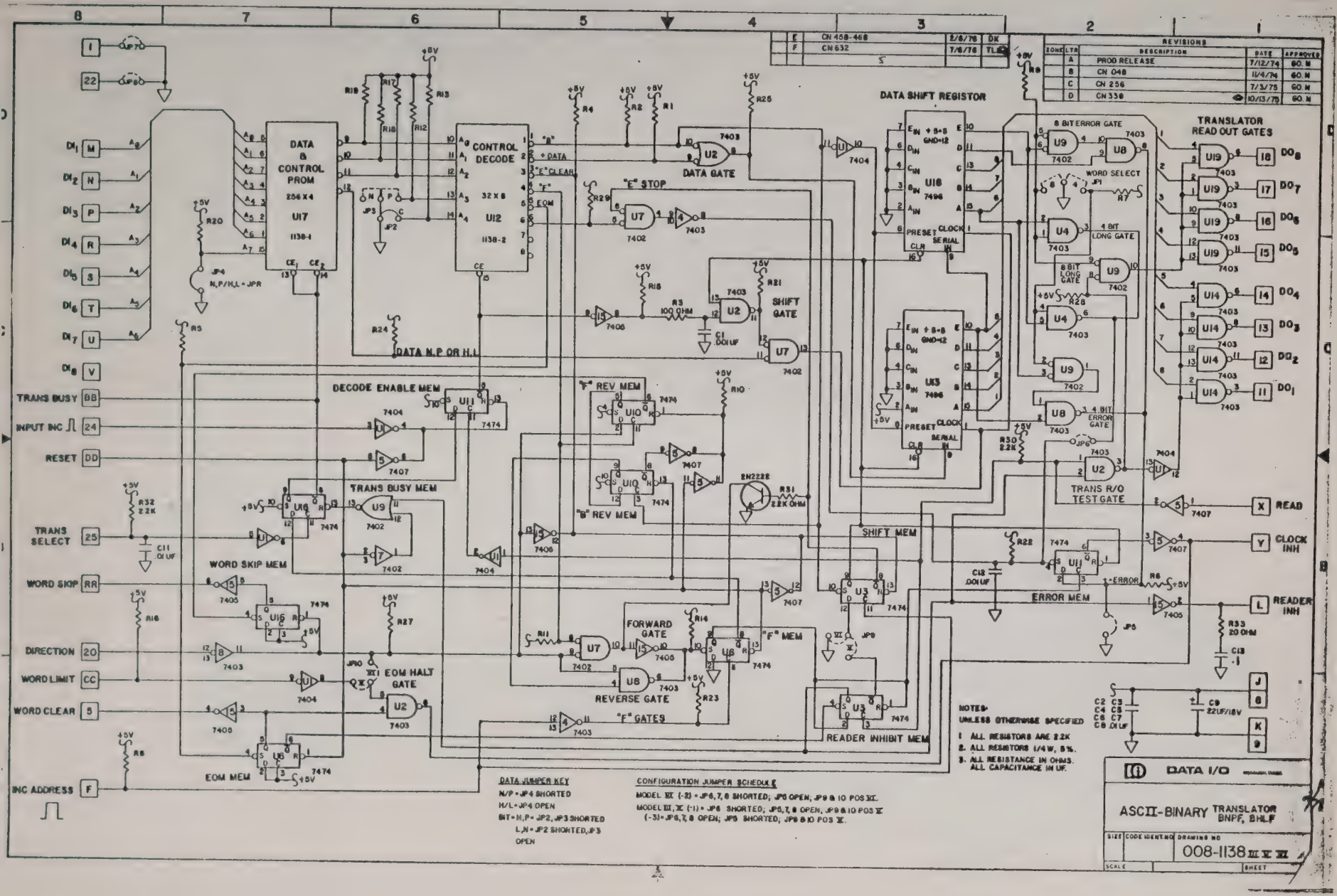
STANDARD PN FORMAT = 1138-1, 1138-2
SPECTRUM FORMAT = 1138-2, 1138-3

1138-3 U17 SPECTRUM FORMAT

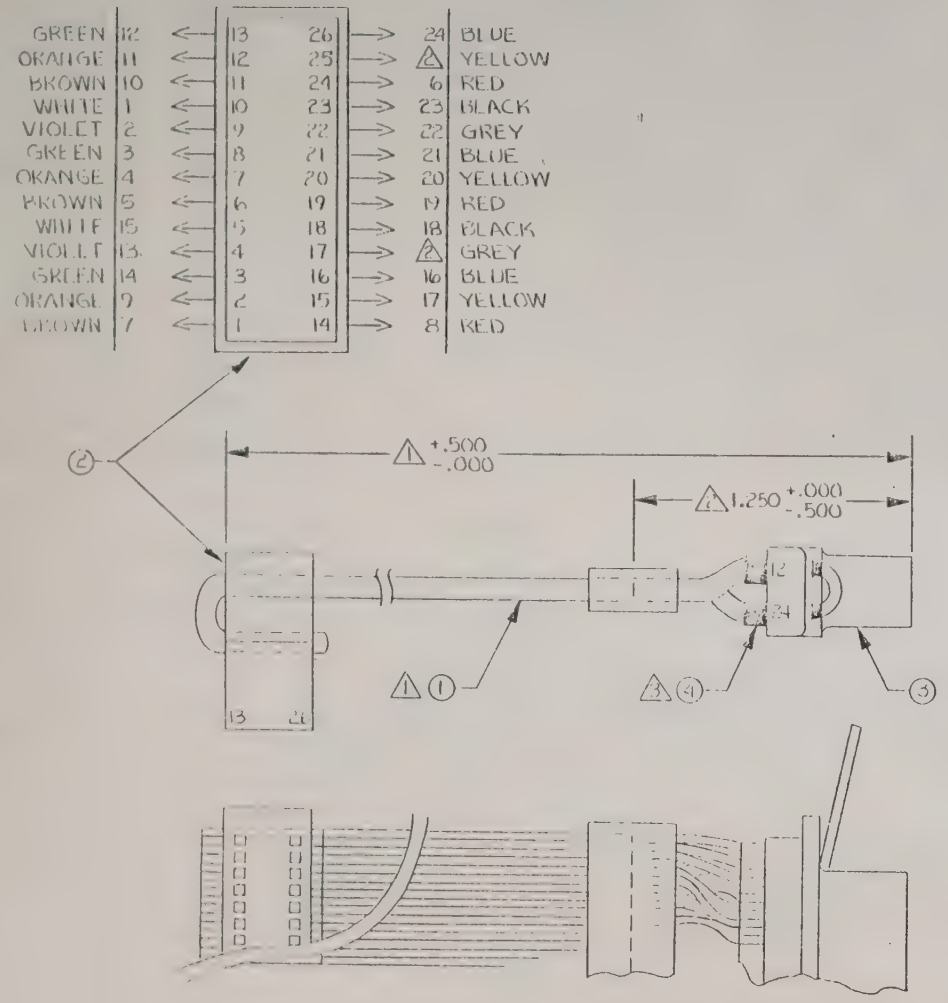
INPUT CHARACTER	DECIMAL "4" 9	"3" 10	"2" 11	"1" 12
SPACE (B) 95,223	1	Ø	Ø	1
Ø (N) 79,207	Ø	1	Ø	Ø
1 (P) 78,206	Ø	Ø	Ø	Ø
C/R (F) 114,242	1	Ø	1	1
NULL 0,128	1	1	Ø	1
DELETE 127,255	1	1	Ø	1

2/28

TOLERANCES (EXCEPT AS NOTED)	DATA I/O REDMOND, WASH.	
DECIMAL ±	TITLE TIMING DIAG	SCALE
FRACTIONAL ±	ASCII — BINARY TRANSLATION	
ANGULAR	DATE	DRAWING NUMBER 007-1138


DATA & CONTROL PROM 256 X 4 U17 1138-1
CONTROL DECODE 32 X 8 U12 1138-2
DATA SHIFT REGISTOR
DATA GATE
"E" STOP
SHIFT GATE
DATA M,P OR H,L
DECODE ENABLE MEM
TRANS BUSY MEM
WORD SKIP MEM
EOM MEM
"E" REV MEM
"B" REV MEM
FORWARD GATE
REVERSE GATE
EOM HALT GATE
"F" GATES
"F" MEM
SHIFT MEM
ERROR MEM
READER INHIBIT MEM
8 BIT ERROR GATE
WORD SELECT
4 BIT LONG GATE
8 BIT LONG GATE
4 BIT ERROR GATE
TRANS R/O TEST GATE
TRANSLATOR READ OUT GATES
DI1 M
DI2 N
DI3 P
DI4 R
DI5 S
DI6 T
DI7 U
DI8 V
TRANS BUSY BB
INPUT INC 24
RESET DD
TRANS SELECT 25
WORD SKIP RR
DIRECTION 20
WORD LIMIT CC
WORD CLEAR 5
INC ADDRESS F
READ X
CLOCK INH Y
READER INH L
DO8 18
DO7 17
DO6 16
DO5 15
DO4 14
DO3 13
DO2 12
DO1 11
NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 2.2K
2. ALL RESISTORS 1/4 W, 5%.
3. ALL RESISTANCE IN OHMS. ALL CAPACITANCE IN UF.
DATA JUMPER KEY
N/P = JP4 SHORTED
H/L = JP4 OPEN
BIT = H,P = JP2, JP3 SHORTED
L,N = JP2 SHORTED, JP3 OPEN
CONFIGURATION JUMPER SCHEDULE
MODEL III (-2) = JP6,7,8 SHORTED; JP5 OPEN; JP9 & 10 POS III.
MODEL III, II (-1) = JP5 SHORTED; JP6,7,8 OPEN, JP9 & 10 POS II
(-3) = JP6,7,8 OPEN; JP5 SHORTED; JP9 & 10 POS II.
DATA I/O
ASCII-BINARY TRANSLATOR BNPF, BHLF
008-1138 III II XII

DATE	BY	REVISION RECORD	DR	CK
12/9	KL	ECN # 1984	KL	

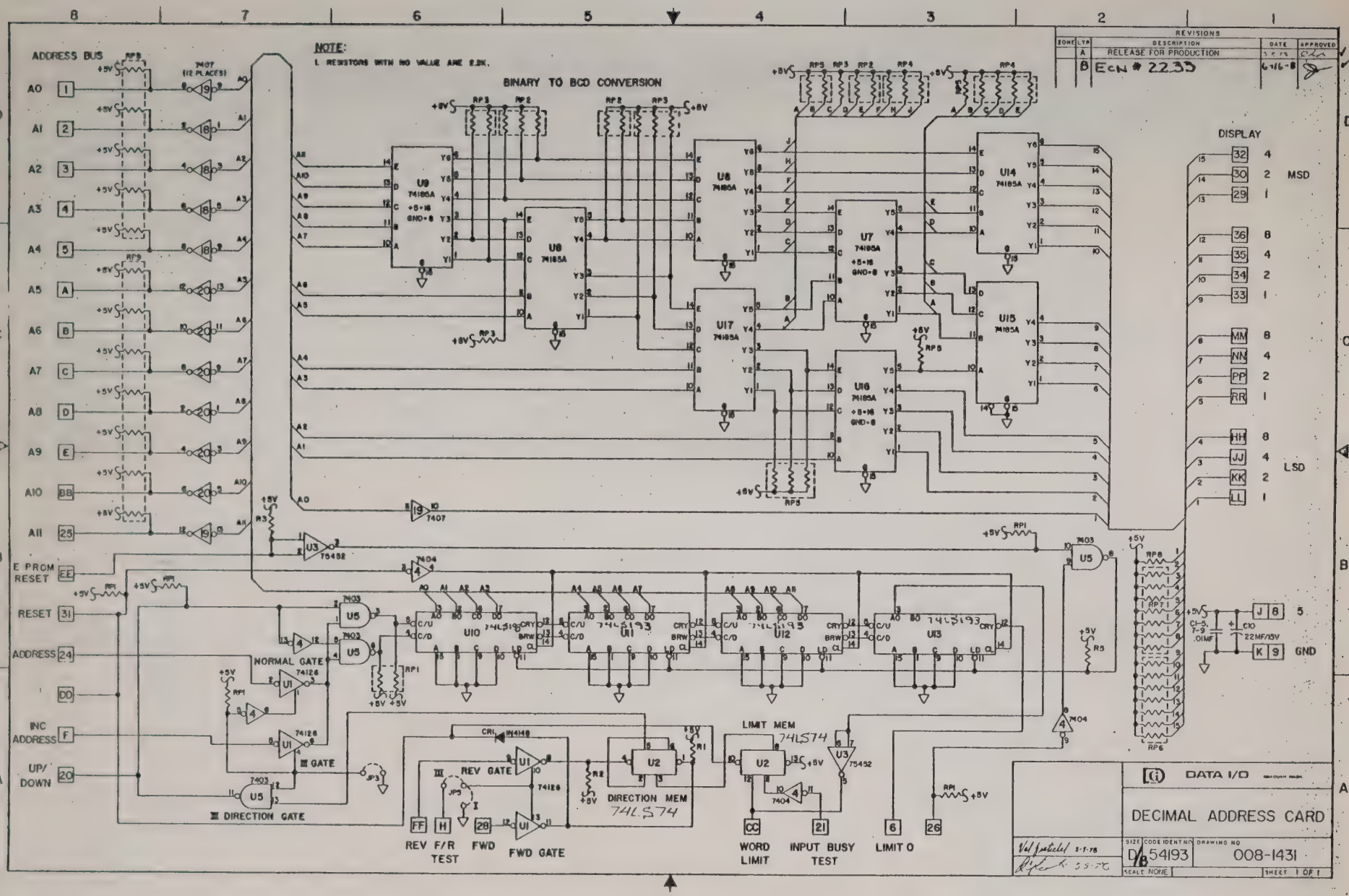


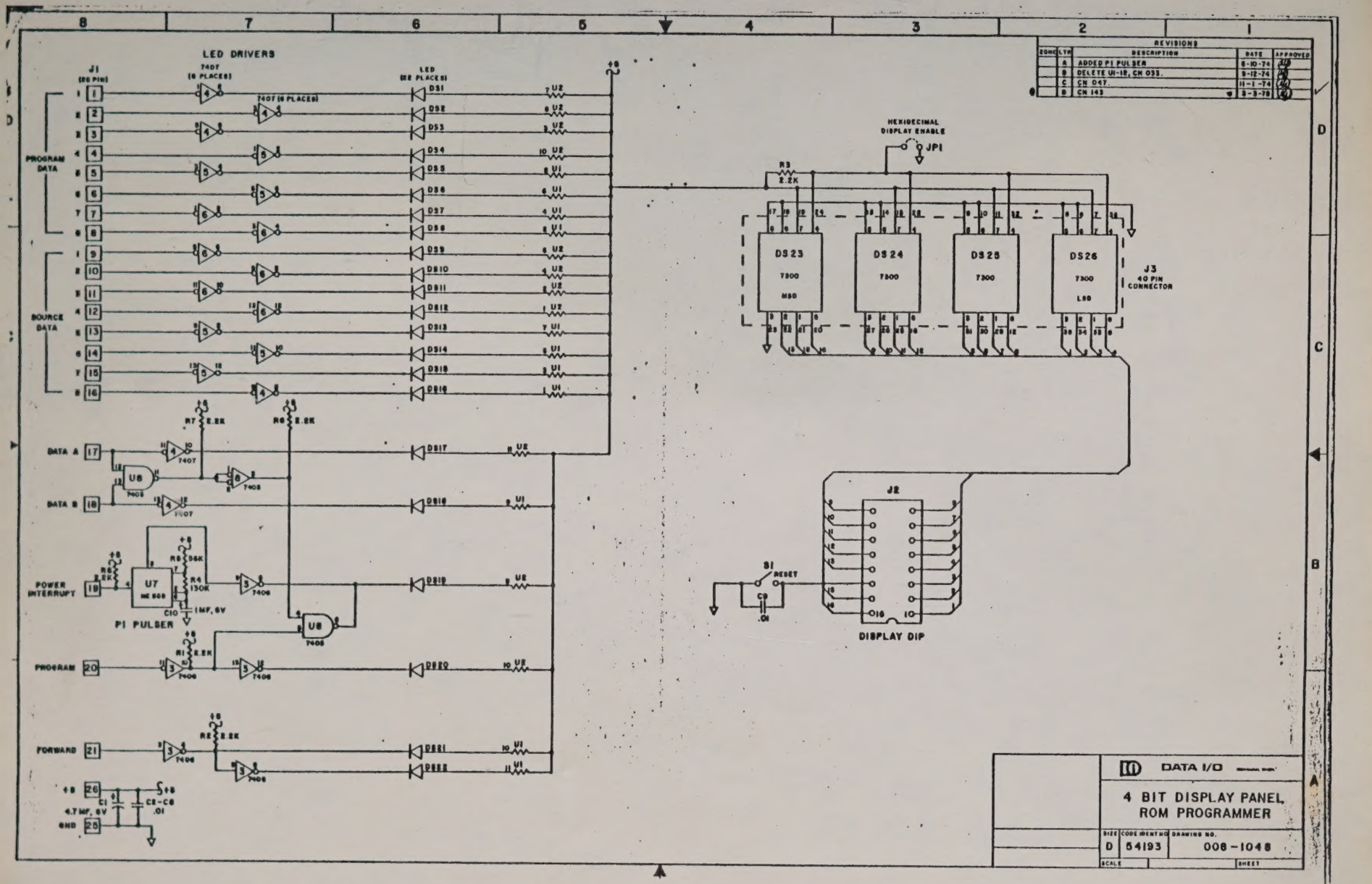
NOTES:

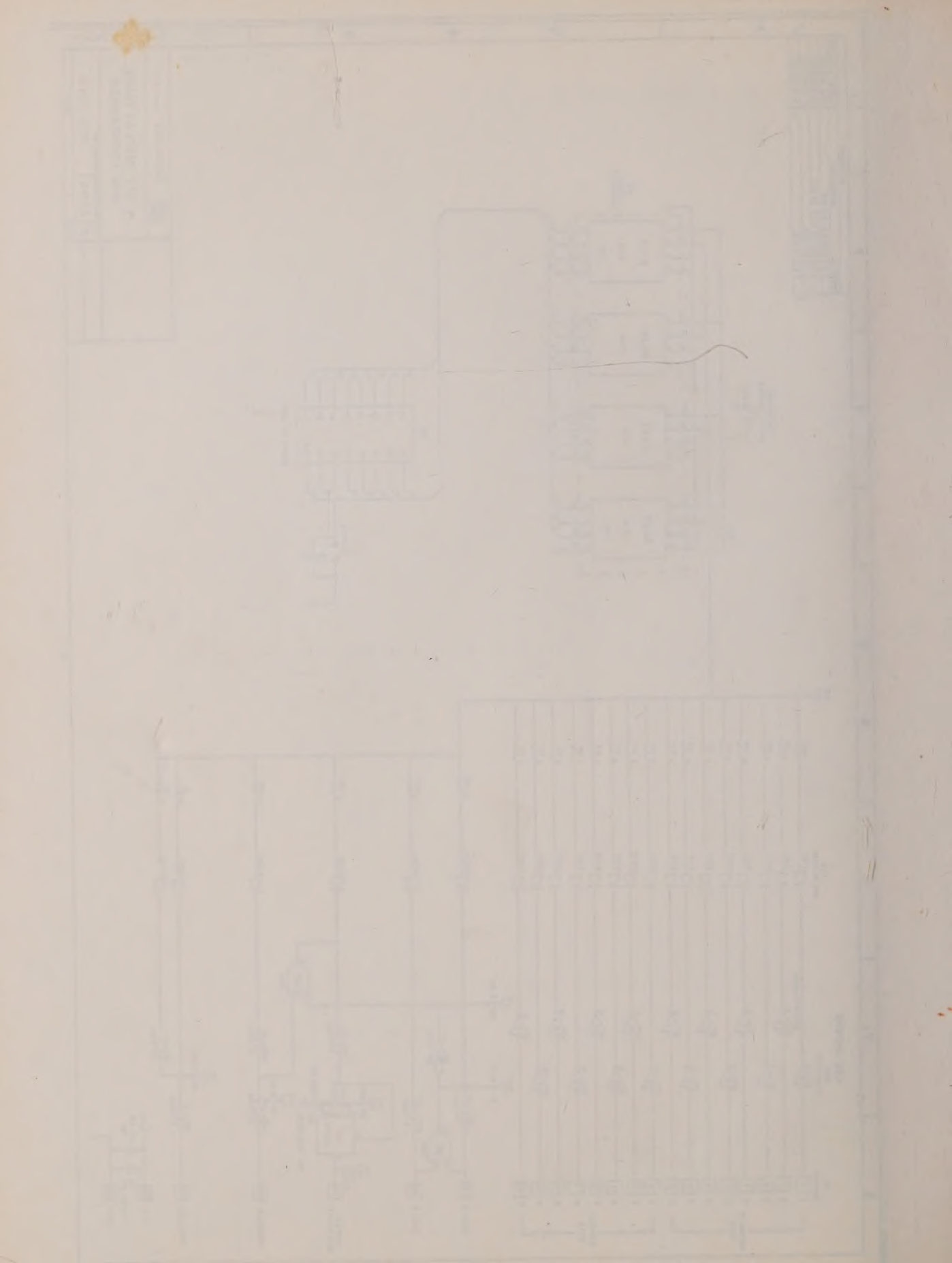
1. LENGTH OF CABLE IS SPECIFIED BY THE LAST TWO DIGITS OF THE PART NUMBER, i.e. 709-1139-10 SPECIFIES A 10 INCH CABLE LENGTH.
2. TRIM UNUSED WIRES NO. 17 AND 25 FROM ITEM (2) AND SECURE WITH TWO COMPLETE WRAPS OF VINYL TAPE. AS DIMENSIONED.
3. SOLDER AND PROTECT WITH ITEM (4).
4. USE BLACK INK TO MARK PART NO. ON FLAT SIDE OF CABLE.

ITEM	QTY	PART NO.	DESCRIPTION
4	AR	525-1500	TUBING, SHRINK
3	1	401-3062	CONNECTOR (24 COND)
2	1	401-1306	CONNECTOR (26 COND)
1	1	408-1291	CABLE (26 COND) FLAT (COLOR CODED)

TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH.		
DECIMAL ± NOTED		SCALE NONE	DRAWN BY K. LANZ
FRACTIONAL ±	TITLE I/O CABLE		APPROVED BY K. Jones
ANGULAR ±	DATE 1-20-78	DRAWING NUMBER 709-1139 4	


NOTE:
1. RESISTORS WITH NO VALUE ARE 2.2K.
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | RELEASE FOR PRODUCTION
B | ECN # 2235
ADDRESS BUS
BINARY TO BCD CONVERSION
DISPLAY
MSD
LSD
NORMAL GATE
III GATE
III DIRECTION GATE
REV F/R TEST
FWD
FWD GATE
DIRECTION MEM
74LS74
LIMIT MEM
74LS74
WORD LIMIT
INPUT BUSY TEST
LIMIT O
E PROM RESET
RESET
ADDRESS
INC ADDRESS
UP/ DOWN
GND
DATA I/O
DECIMAL ADDRESS CARD
SIZE B
CODE IDENT NO 54193
DRAWING NO 008-1431
SCALE NONE
SHEET 1 OF 1


LED DRIVERS
J1
(20 PIN)
7407
(6 PLACES)
LED
(22 PLACES)
PROGRAM DATA
SOURCE DATA
DATA A
DATA B
POWER INTERRUPT
PROGRAM
FORWARD
GND
P1 PULSER
U7
NE 555
HEXIDECIMAL DISPLAY ENABLE
JP1
R3
2.2K
DS23
DS24
DS25
DS26
7300
J3
40 PIN CONNECTOR
J2
DISPLAY DIP
S1
RESET
C9
.01
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
A
ADDED P1 PULSER
8-10-74
B
DELETE U1-16, CN 033.
9-12-74
C
CN 047.
11-1-74
D
CN 143
3-3-75
DATA I/O
4 BIT DISPLAY PANEL
ROM PROGRAMMER
SIZE
D
CODE IDENT NO
54193
DRAWING NO.
008-1048
SCALE
SHEET



DATA I/O

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